

Title Page

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Project Name

CPUC_DVN-0619-ZZ

Revision

- R0A
- > First Initial
- R0B
- > 115200000362A NMOS Phase Out
 - > Change Q3, Q6 to 115200000312A
 - > MAX16507 default scenario is wrong
 - > Change R29 to 20013020BN60A (13k ohm)
 - > Change R417 to 20017420FN60A (17.4k ohm)
 - > Add diode for external flashing EC SPI
 - > Add D30 and reserved L31
 - > Add diode for EC quick shutdown
 - > Add D31 for EC_WRST_N discharge route
 - > Modify P3V30A power switch MOS soft-start
 - > Change C275 to MOS gate side
 - > Change R502 to 200500000047A (1k ohm, 0402, 0.1%)
 - > X1 Crystal frequency tuning (32.768kHz)
 - > Change C79,C81 to 204700000090A (15pF, 0402)
 - > Change X1 to 116000000339A (ETST00327000XE)
 - > X2 Crystal frequency tuning (25MHz)
 - > Change C98,C99 to 204000000159H (27pF, 0402)
 - > Fix 10GbE RBIAS Resistor
 - > Change R546,R548 to 200500000047A (1k ohm, 0402, 0.1%)
 - > Change CPU Part Number
 - > Change U9 to 110000000610A (non-project part)
 - > ESPI_EN# is required pull up at module
 - > Add R705 for pull up (20k ohm, 200500001698A)
 - > EC GPC3 Switch
 - > Add R706 for testing (0 ohm, 200000000JN60A)
 - > Modify 5VSB power switch MOS soft-start
 - > Change C381 to MOS gate side
 - > Change R553 to 200500000047A (1k ohm, 0402, 0.1%)
 - > VCCRAM Jitter Issue
 - > Add C453 at bottom side (100uF, 204000000569A)
 - > Remove I210 SMBUS Connection
 - > Change R314,R323,R324 to placed
 - > Change R312,R322,R329 to DNP
 - > Change LED's brightness
 - > Add Q10,Q11,Q12,Q13,Q14,Q15,Q16,Q17 for MOS driving (115200000312A)
 - > Change R5,R6,R7,R8,R9,R10,R12,R13 to 20022000FN60E (220 ohm)
 - > Change LED1,LED2,LED3,LED4,LED5,LED6,LED7,LED8 to 115100000085A

Project Part Numbers

- | | |
|---------------|--|
| FP3ZZCOME001A | ??SWITCH CPUC_DVN-0619-ZZ , 1 N |
| PP3ZZCOME001A | ??SHIP KIT CPUC_DVN-0619-ZZ |
| CP3ZZCOME001A | ??CONFIG CPUC_DVN-0619-ZZ |
| NP3ZZCOME002A | ??PCBA CPUC_DVN-0619-ZZ CPU MODULE |
| SP3ZZCOME002A | ??SMD ASM CPUC_DVN-0619-ZZ CPU MODULE |
| TP3ZZCOME002A | ??NON SMD ASM CPUC_DVN-0619-ZZ CPU MODULE |
| 142000002428A | ??R0A PCB 16L CPUC_DVN-0619-ZZ CPU OSP+G |
| 165000002287A | RNA SCHEMATIC FILE CPUC_DVN-0619-ZZ CPU MODULE |
| WP3ZZCOME007A | ??F/W ASM CPUC_DVN-0619-ZZ U19(BIOS) (OFF-LINE) |
| WP3ZZCOME008A | ??F/W ASM CPUC_DVN-0619-ZZ -U30(EC) (OFF-LINE) |
| WP3ZZCOME009A | ??F/W ASM CPUC_DVN-0619-ZZ -U35(I210) (OFF-LINE) |
| 249100004653A | RNA F/W EEPROM CPUC_DVN-0619-ZZ U19(BIOS) |
| 249100004654A | RNA F/W EEPROM CPUC_DVN-0619-ZZ -U30(EC) |
| 249100004652A | RNA F/W EEPROM CPUC_DVN-0619-ZZ -U35(I210) |

- R0B
- > 10G LED I2C need pull up
 - > Add R707,R708 for pull up (4.7k, 20047010FN60A)
 - > EC will detect high when COME_PWR_OK is floating
 - > Remove TP19 and add R709 for pull down (100k, 20010030FN61E)
 - > Reserved R710 for pull up
 - > Change mounting hole to OSP type
 - > Change H1,H2,H3,H4,H5 footprint to mth_236c106d_8dp_osp

Parts Value Annotation

@:	not stuffed	/6.3V: 6.3V rated voltage	/120Z: 120 ohm impedance at 100 MHz
/4:	0402 size	/10V: 10V rated voltage	/5%: 5% tolerance
/6:	0603 size	/25V: 25V rated voltage	/1%: 1% tolerance
/8:	0805 size	/50V: 50V rated voltage	/0.1%: 0.1% tolerance
/12:	1206 size	/6A: 6A rated current	
/1210:	1210 size	/X5R: X5R type MLCC	
		/X7R: X7R type MLCC	
		/NPO: NPO type MLCC	

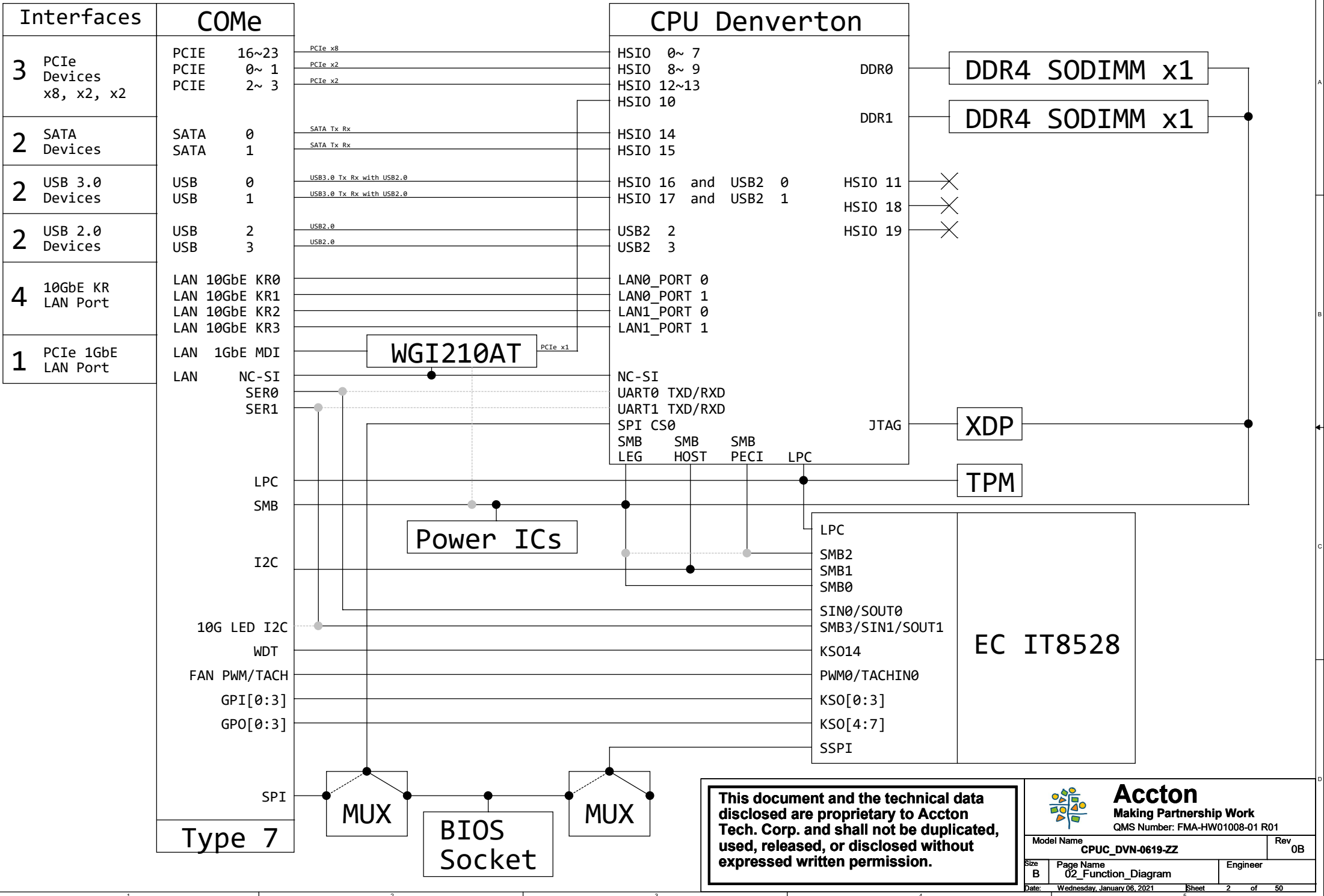
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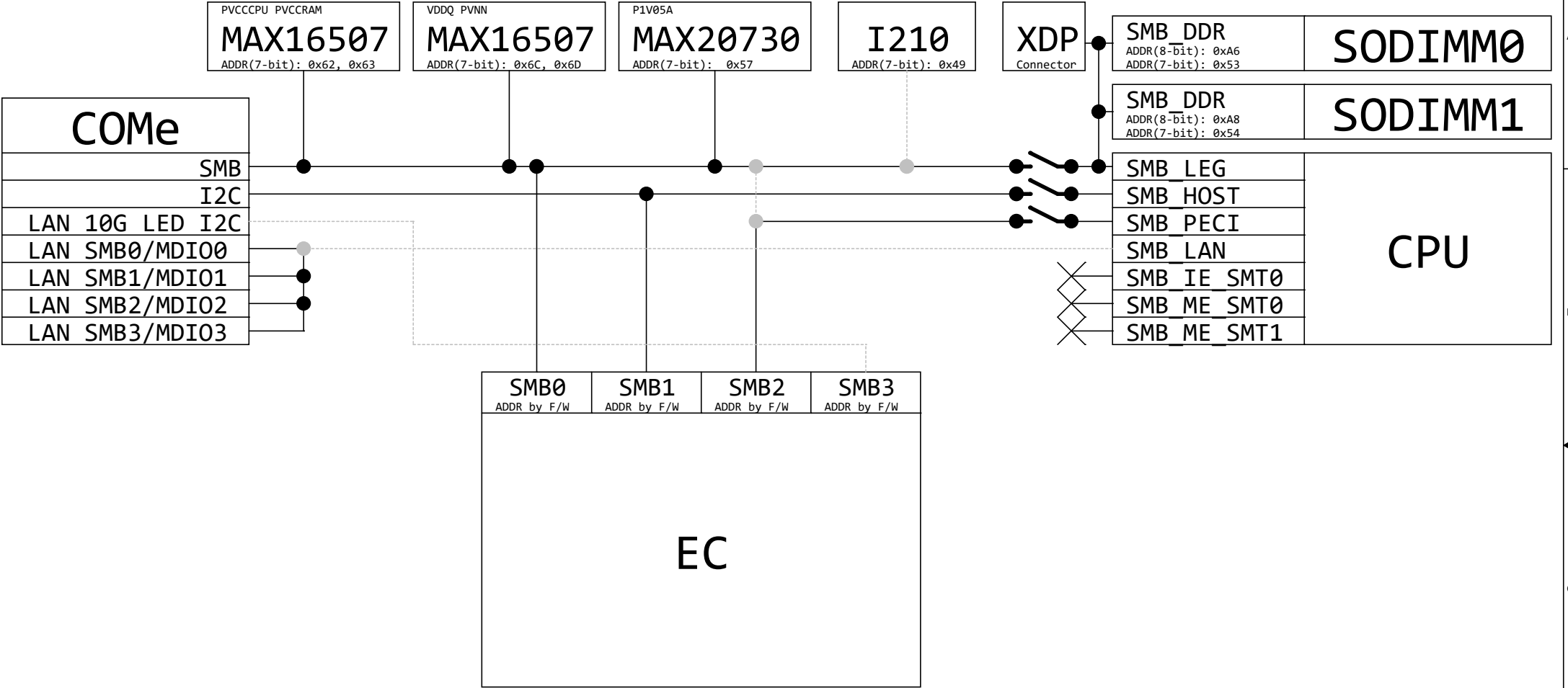
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Function Diagram



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SMBUS I2C Diagram



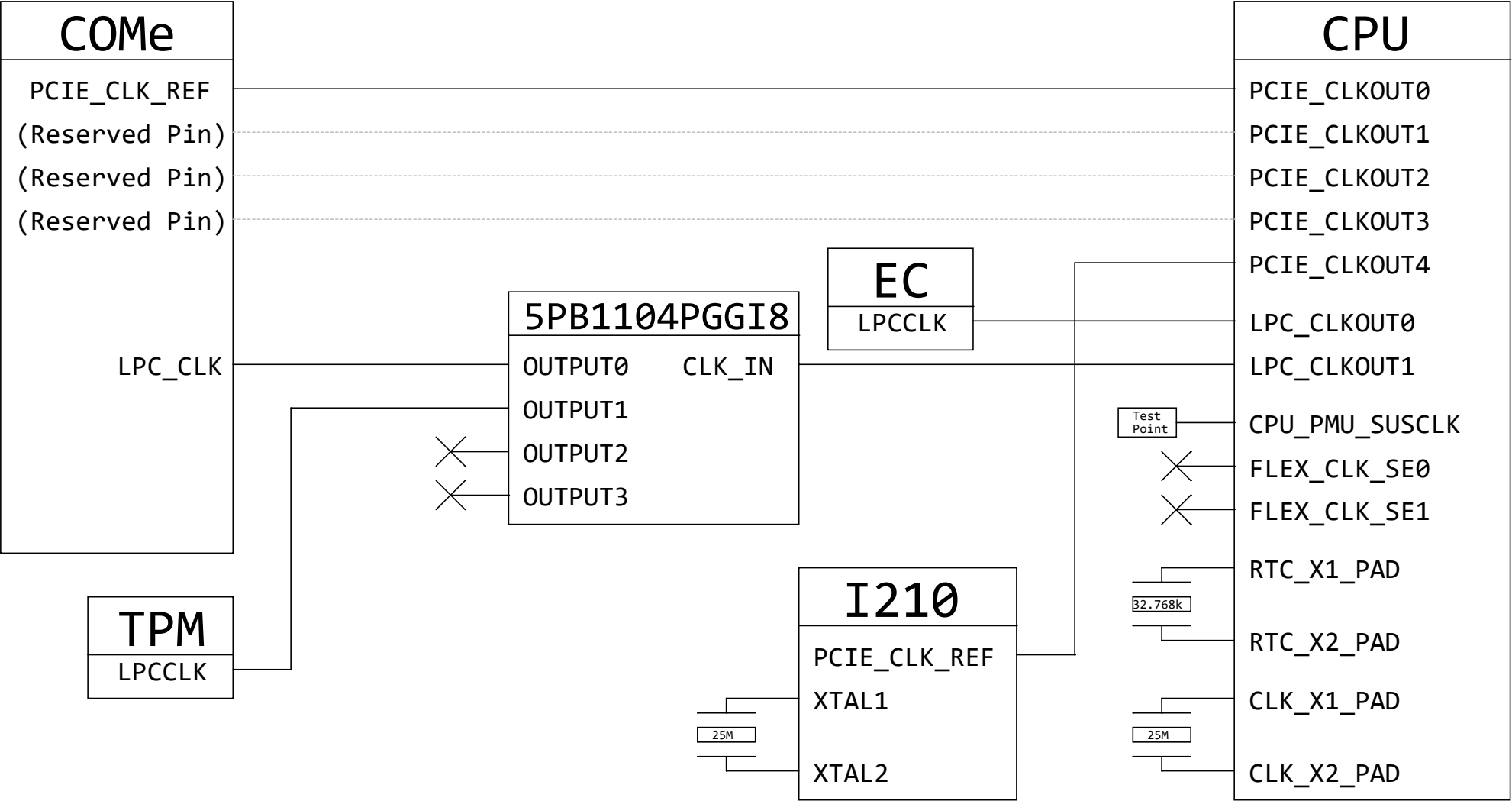
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A	03_SMBUS_I2C_Diagram	
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Clock Diagram



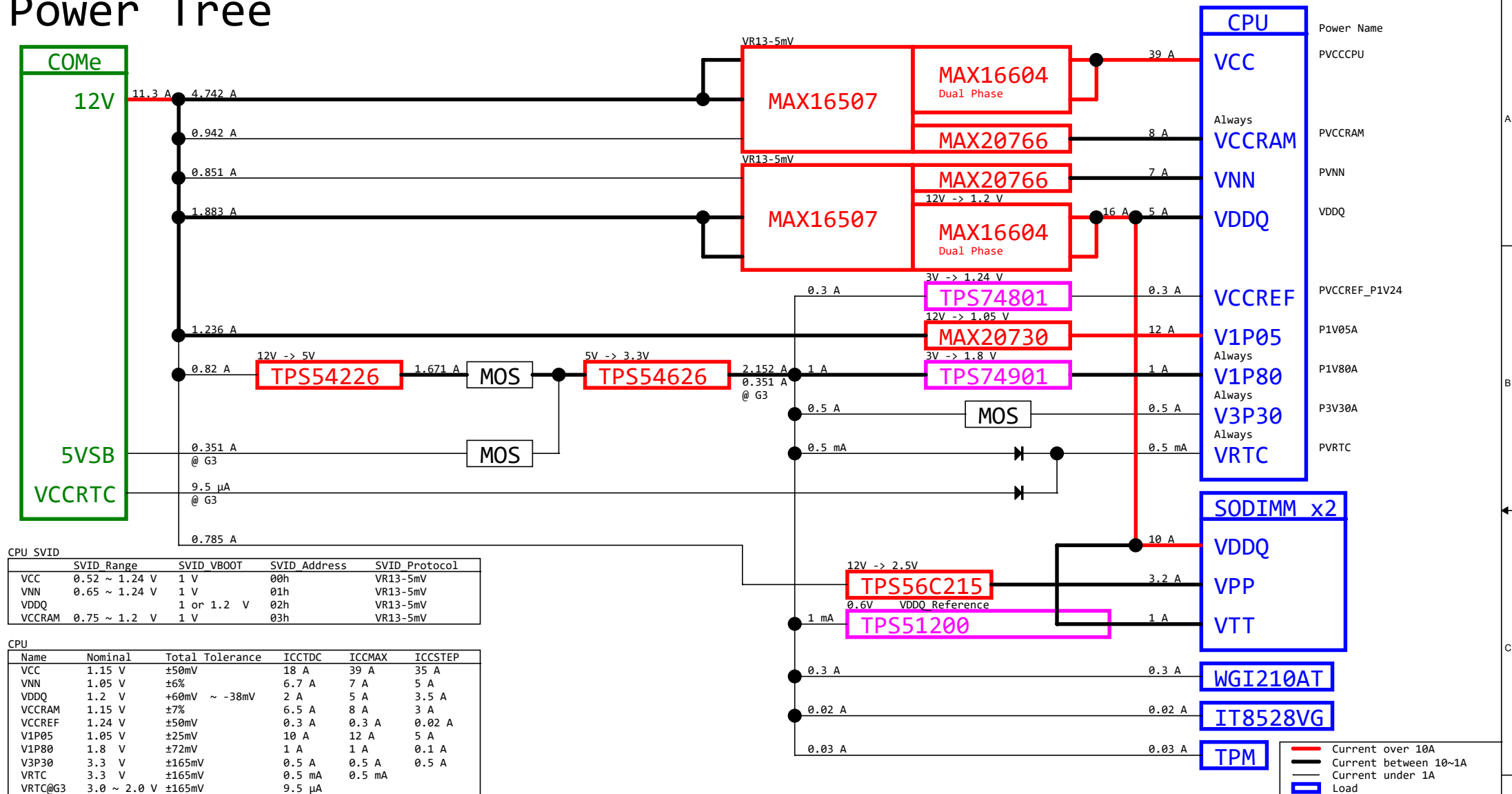
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Power Tree



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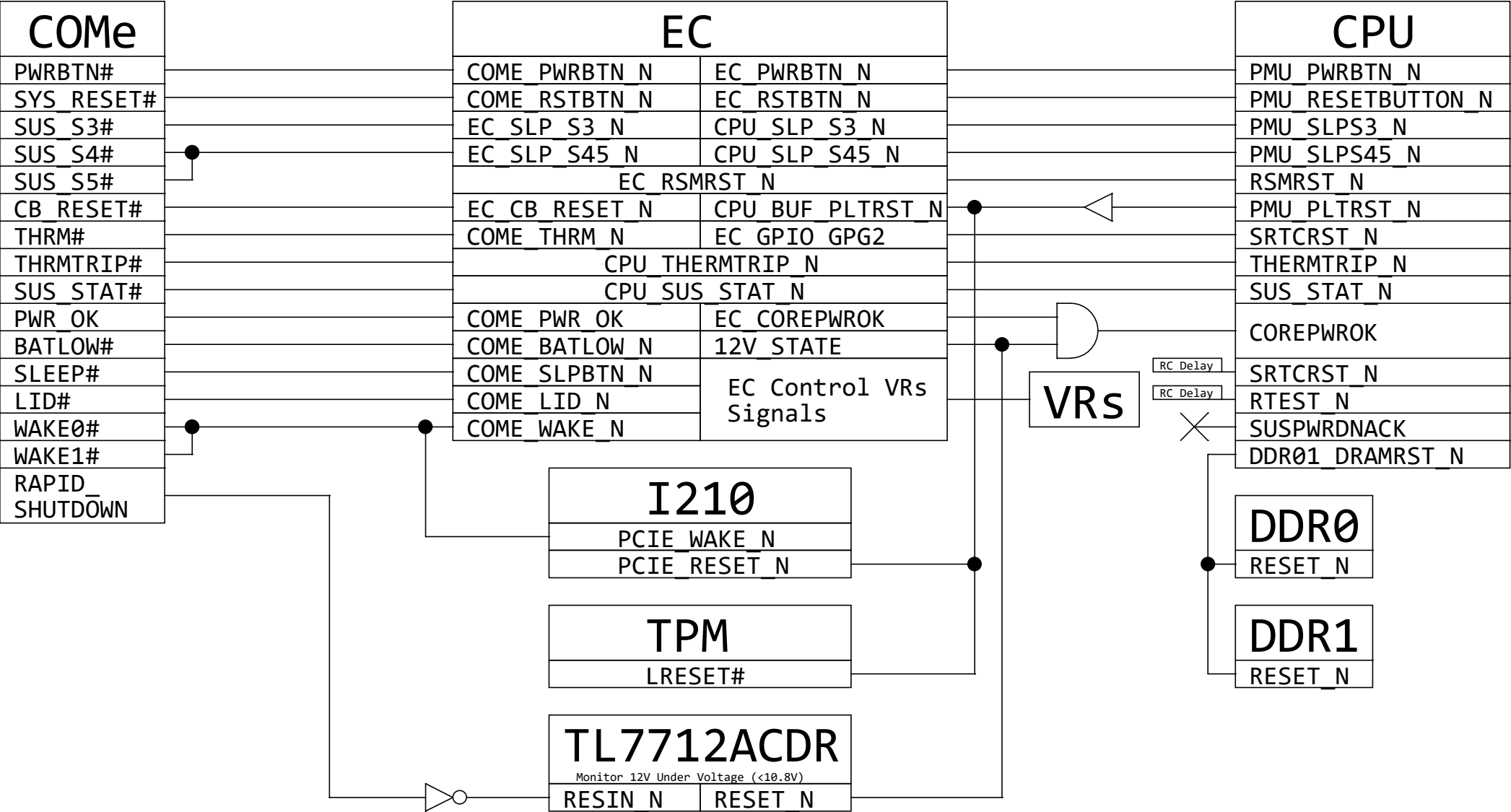
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A	05_Power_Tree			
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Reset Block Diagram



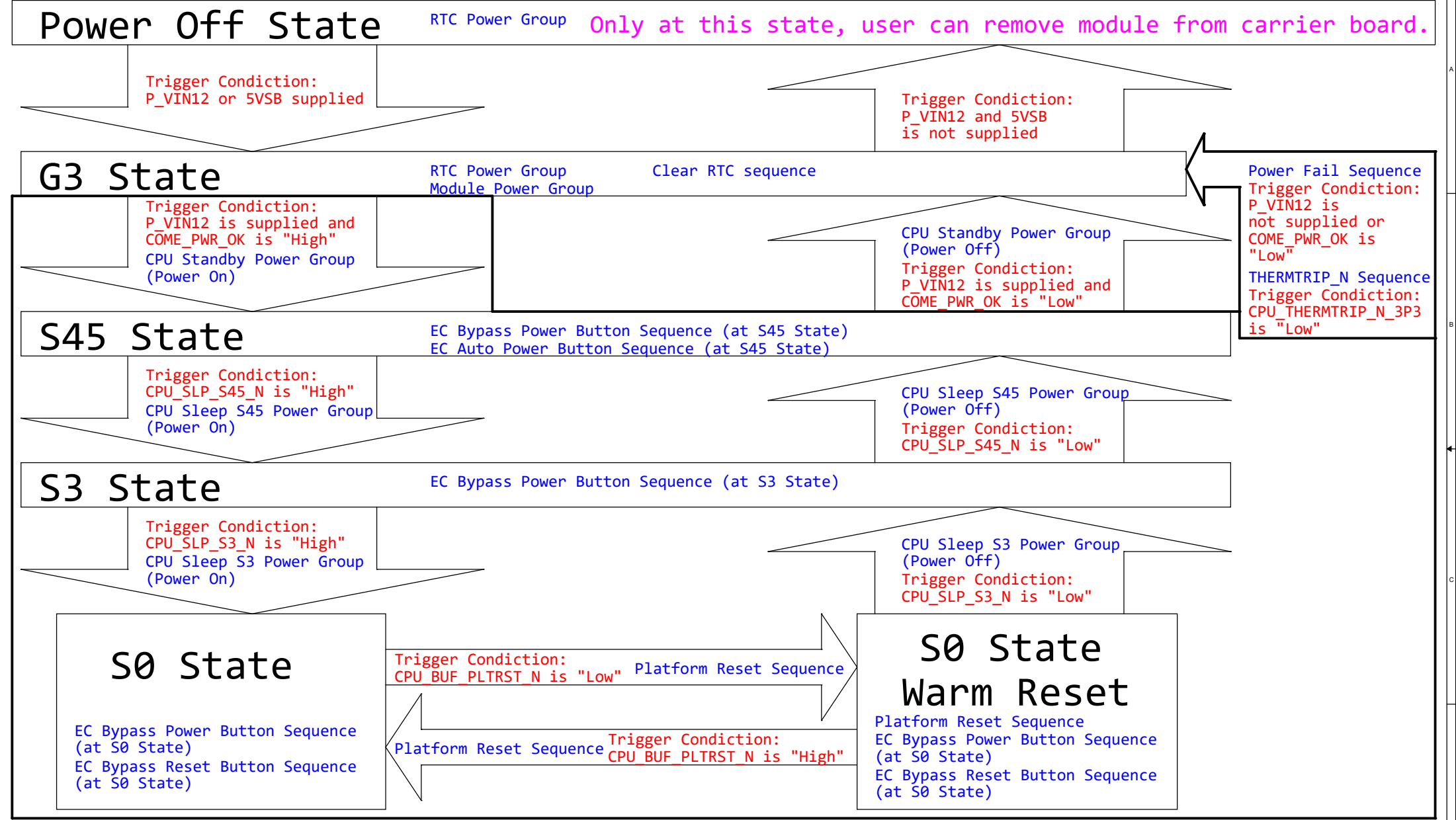
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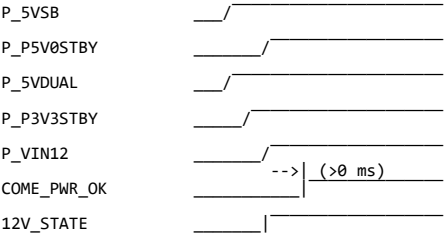
Power State Diagram



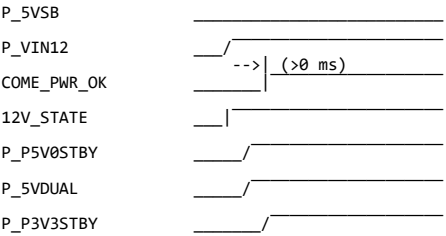
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Module Power Sequence

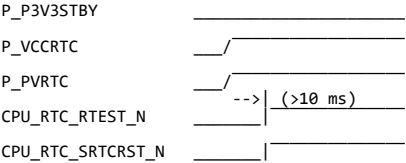
Module Power Group (Power On with 5VSB)



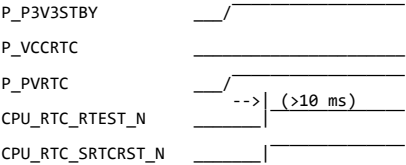
Module Power Group (Power On without 5VSB)



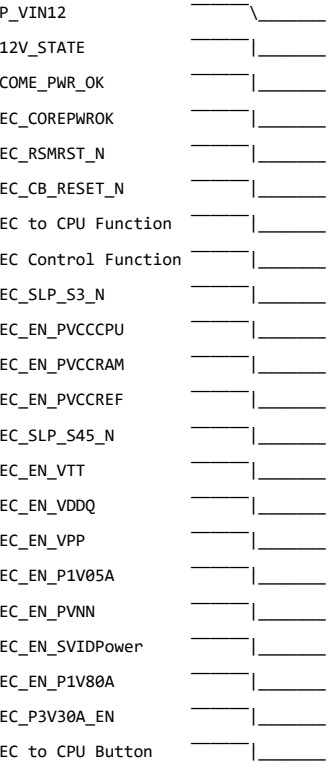
RTC Power Group (Power On with Battery)



RTC Power Group (Power On without Battery)



Power Fail Sequence

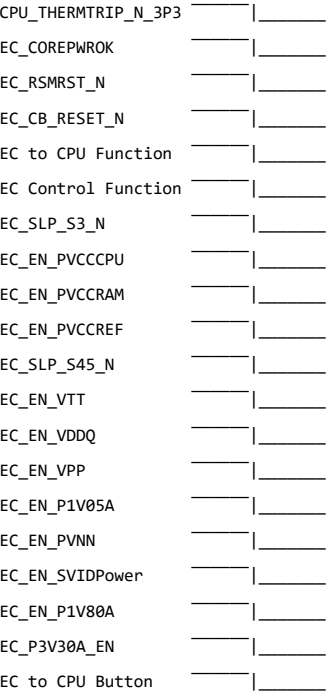


EC to CPU Button Group:
EC_PWRBTN_N
EC_RSTBTN_N

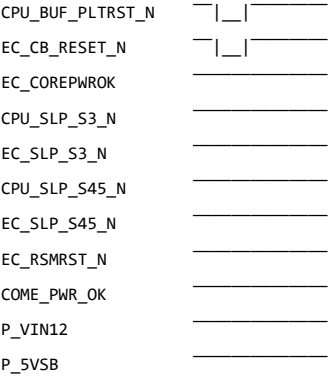
EC to CPU Function Group:
EC_NMI_N
EC_SCI_N
EC_SMI_N

EC Control Function Group:
EC_LPC_EN
EC_USB_EN
EC_EN_CPU_SMB_LEG
EC_EN_CPU_SMB_HOST
EC_EN_CPU_SMB_PECI

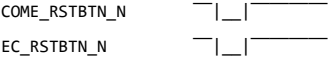
THERMTRIP_N Sequence



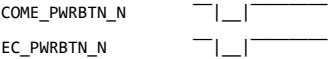
Platform Reset Sequence



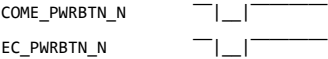
EC Bypass Reset Button Sequence (at S0 State)



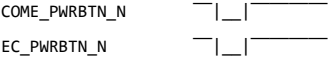
EC Bypass Power Button Sequence (at S0 State)



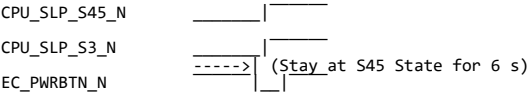
EC Bypass Power Button Sequence (at S3 State)



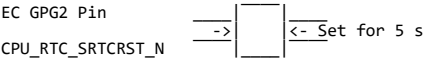
EC Bypass Power Button Sequence (at S45 State)



EC Auto Power Button Sequence (at S45 State)



EC Clear RTC Sequence (at G3 State)



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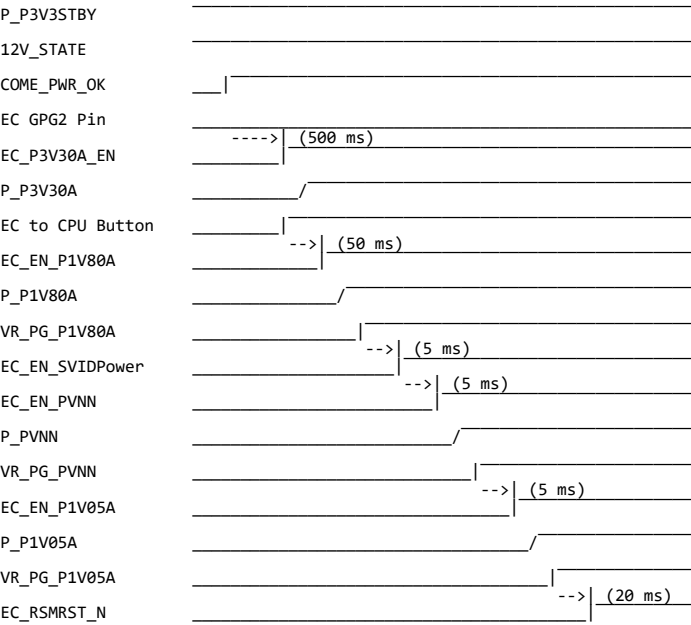
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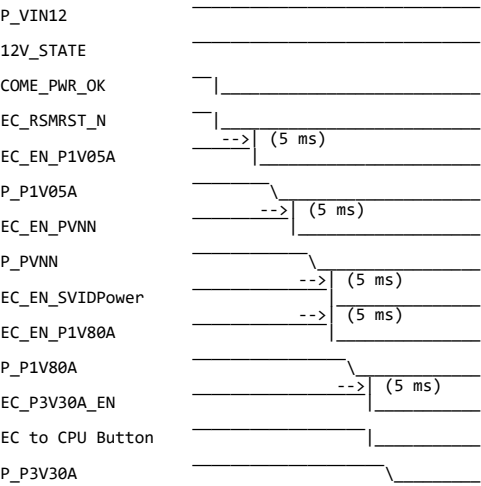
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CPU Power Sequence

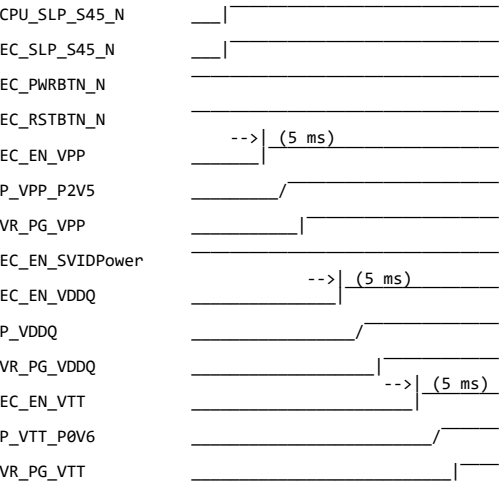
CPU Standby Power Group (Power On)



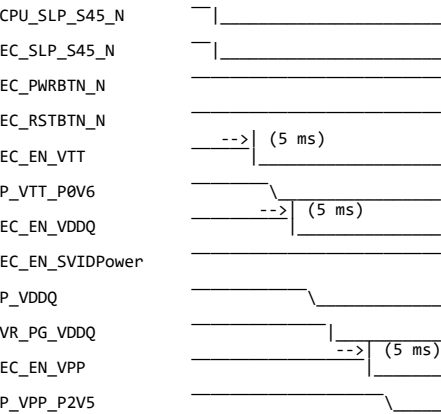
CPU Standby Power Group (Power Off)



CPU Sleep S45 Power Group (Power On)



CPU Sleep S45 Power Group (Power Off)



EC to CPU Button Group:

EC_PWRBTN_N
EC_RSTBTN_N

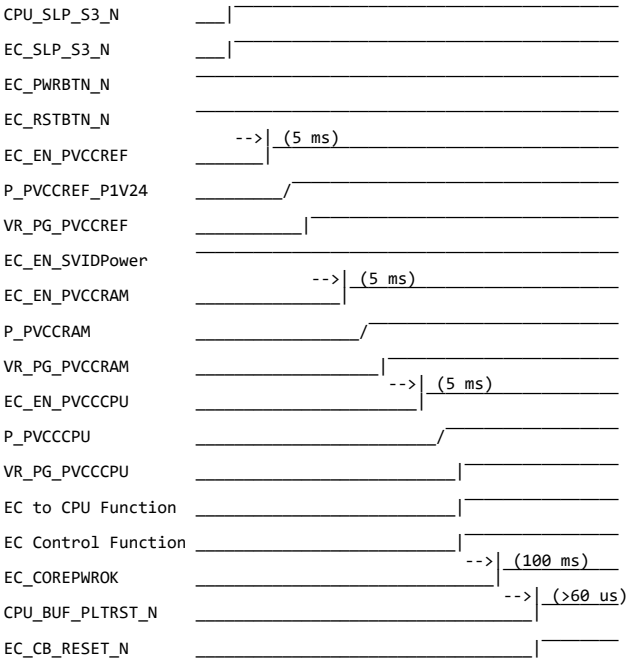
EC to CPU Function Group:

EC_NMI_N
EC_SCI_N
EC_SMI_N

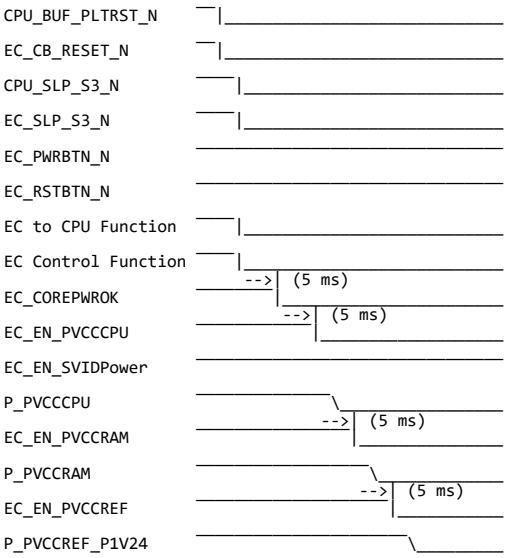
EC Control Function Group:

EC_LPC_EN
EC_USB_EN
EC_EN_CPU_SMB_LEG
EC_EN_CPU_SMB_HOST
EC_EN_CPU_SMB_PECI

CPU Sleep S3 Power Group (Power On)



CPU Sleep S3 Power Group (Power Off)



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EC Pin Define

Pin	Main Function	Net Name	Description
GPA0	PWM	EC_FAN_PWMOUT	Carrier fan PWM function.
GPA1	GPIO Output	EC_NMI_N	EC output to CPU NMI_N signal. Low Active.
GPA2	GPIO Input	VR_PG_PVCCREF	PVCCREF power good signal. "High" indicating PVCCREF power is ready.
GPA3	GPIO Output	EC_EN_PVCCRAM	PVCCRAM power enable signal. Set "High" to enable PVCCRAM power. Required set EC_EN_SVIDPOWER to "High" before set EC_EN_PVCCRAM to "High".
GPA4	GPIO Output	EC_EN_PVNN	PVNN power enable signal. Set "High" to enable PVNN power. Required set EC_EN_SVIDPOWER to "High" before set EC_EN_PVNN to "High".
GPA5	GPIO Output	EC_PWRBTN_N	EC output to CPU power button signal. Low Active.
GPA6	GPIO Output*	SPI_EC_SSCK	EC output to CPU PCIE_CLKREQ04_N signal. Set "High" to disable CPU PCIE_CLKOUT4. Alternative Function is SSPI interface.
GPA7	GPIO Output	EC_EN_PIV05A	PIV05A power enable signal. Set "High" to enable PIV05A power.
GPB0	COM Port	EC_SER0_RX	EC COM Port RX function. Connect to carrier SER0.
GPB1	COM Port TX	EC_SER0_TX	EC COM Port TX function. Connect to carrier SER0.
GPB2	GPIO Input	COME_SLPBTN_N	Carrier SLPBTN_N output signal. Active Low.
GPB3	SMBUS	SMB_CLK	EC SMB interface. H/W Default is connected to CPU SMB_LEG, DDR SMBus and carrier SMBus interface. Required set EC_EN_CPU_SMB_LEG to "High" for CPU SMB_LEG and DDR SMB access.
GPB4	SMBUS	SMB_DATA	EC SMB interface. H/W Default is connected to CPU SMB_LEG, DDR SMBus and carrier SMBus interface. Required set EC_EN_CPU_SMB_LEG to "High" for CPU SMB_LEG and DDR SMB access.
GPB5	N/A	EC_GA20	Reserved.
GPB6	N/A	EC_KBRST_N	EC Reset Pin. Reserved.
GPB7	GPIO Output	EC_RSMRST_N	EC output to CPU RSMRST_N signal. "High" indicating CPU standby power group is ready.
GPC0	GPIO Output	EC_EN_PVCCREF	PVCCREF Power enable signal. Set "High" to enable PVCCREF power.
GPC1	SMBUS	I2C_EC_CLK	EC SMB interface. H/W Default is connected to CPU SMB_HOST and carrier I2C. Required set EC_EN_CPU_SMB_HOST to "High" for CPU SMB_HOST access.
GPC2	SMBUS	I2C_EC_DAT	EC SMB interface. H/W Default is connected to CPU SMB_HOST and carrier I2C. Required set EC_EN_CPU_SMB_HOST to "High" for CPU SMB_HOST access.
GPC3	GPIO Input*	SPI_EC_SMOSI	H/W DIP switch input High/Low. Reserved for S/W. Alternative Function is SSPI interface.
GPC4	GPIO Input	CPU_SLP_S3_N	CPU output to EC SLP_S3_N signal. "High" indicating sleep S3 power group should be enabled.
GPC5	GPIO Input	SPI_EC_SMISO	SVID VR output VR_SVIDPOWER_ALERT_N signal. "Low" indicating SVID power group have fail event. Alternative Function is SSPI interface.
GPC6	GPIO Input	VR_PG_PVCCRAM	PVCCRAM power good signal. "High" indicating PVCCRAM power is ready.
GPC7	GPIO Output	EC_P3V30A_EN	P3V30A power enable signal. Set "High" to enable P3V30A power.
GPC8	GPIO Input	VR_PG_VTT	VTT power good signal. "High" indicating VTT power is ready.
GPC9	GPIO Input	COME_WAKE_N	Carrier output WAKE_N signal. Active Low.
GPC10	GPIO Input	CPUEC_PLTRST_N	CPU output to EC PLTRST_N signal. "High" indicating CPU is finished power on sequence.
GPC11	GPIO Output	EC_SCI_N	EC output to CPU SCI_N signal. Low Active.
GPC12	GPIO Output	EC_SMI_N	EC output to CPU SMI_N signal. Low Active.
GPC13	GPIO Output	EC_EN_VPP	VPP power enable signal. Set "High" to enable VPP power.
GPC14	TACHIN	EC_FAN_TACHIN	Carrier fan TACHIN function.
GPC15	GPIO Output	EC_LED_PWR_EN	Module LED enable signal. Set "High" to enable LED.
GPC16	GPIO Input	CPU_THERMTRIP_N_3P3	CPU output to EC and carrier THERMTRIP_N signal. "Low" indicating CPU has a thermal shutdown event.
GPC17	GPIO Output	EC_SLP_S45_N	EC output to carrier SLP_S45_N signal. This pin will echo CPU_SLP_S45_N status.
GPC18	GPIO Input	CPU_SLP_S45_N	CPU output to EC SLP_S45_N signal. "High" indicating sleep S4 power group should be enabled.
GPC19	GPIO Input	COME_LID_N	Carrier output to EC LID_N signal. Active Low.
GPC20	GPIO Input	COME_PWRBTN_N	Carrier output to EC_PWRBTN_N signal. Active Low.
GPC21	GPIO Input	VR_PG_PIV05A	PIV05A power good signal. "High" indicating PIV05A power is ready.
GPC22	GPIO Input	CPUEC_SUS_STAT_N	CPU output to EC SUS_STAT_N signal. Active Low.
GPC23	GPIO Input	COME_THRM_N	Carrier output to EC THRM_N signal. Active Low.
GPC24	GPIO Output	EC_EN_PVCCCPU	PVCCCPU power enable signal. Set "High" to enable PVCCCPU power. Required set EC_EN_SVIDPOWER to "High" before set EC_EN_PVCCCPU to "High".
GPC25	GPIO Input	VR_PG_PVCCCPU	PVCCCPU power good signal. "High" indicating PVCCCPU power is ready.
GPC26	GPIO Input	COME_BIOS_DIS0_N	Carrier output BIOS_DIS0_N signal. Used to modify EC_BIOS_SPI_MUX_SEL setting.
GPC27	GPIO Input	COME_BIOS_DIS1_N	Carrier output BIOS_DIS1_N signal. Used to modify EC_BIOS_SPI_MUX_SEL setting.
GPC28	GPIO Input	I2V_STATE	Carrier 12V under voltage (<10.8V) and carrier RAPID_SHUTDOWN indication. "Low" indicating EC need to quick translation the CPU power state to G3.
GPC29	GPIO Input	EC_CB_RESET_N	EC output to carrier CB_RESET_N. This pin will echo CPU_PLTRST_N status.
GPC30	GPIO Output	EC_SMB_PECI_CLK	EC SMB interface. H/W Default is connected to CPU SMB_PECI. Required set EC_EN_CPU_SMB_PECI to "High" for CPU SMB_PECI access.
GPC31	GPIO Output	SMB_EC_PECI_DAT	EC SMB interface. H/W Default is connected to CPU SMB_PECI. Required set EC_EN_CPU_SMB_PECI to "High" for CPU SMB_PECI access.
GPC32	GPIO Output	EC_EN_VTT	VTT power enable signal. Set "High" to enable VTT power.
GPC33	GPIO Input	VR_PG_PVNN	PVNN power good signal. "High" indicating PVNN power is ready.
GPC34	GPIO Output*	SPI_EC_SSCE_N	EC output to CPU SRTCRST_N signal. Set "High" to clear CPU CMOS setting. This action only can be done at G3 state. Alternative Function is SSPI interface.
GPC35	GPIO Output	EC_COREPWROK	EC output to CPU COREPWROK signal. "High" indicating all power group is ready.
GPC36	GPIO Input	VR_PG_VPP	VPP power good signal. "High" indicating VPP power is ready.
GPC37	GPIO Input	I2C_EC_CLK_SER1_RX	EC COM Port RX function. Connect to carrier SER1. H/W Default is connected to SER1, can change H/W to I0G LED I2C.
GPC38	COM Port*	I2C_EC_DAT_SER1_TX	EC COM Port TX function. Connect to carrier SER1. H/W Default is connected to SER1, can change H/W to I0G LED I2C.
GPC39	GPIO Input	COME_PWR_OK	Carrier output to EC_PWR_OK signal. "High" indicating carrier 12V output power is ready.
GPC40	GPIO Output	EC_RSTBTN_N	EC output to CPU RSTBTN_N signal. Low Active.
GPC41	GPIO Input	COME_RSTBTN_N	Carrier output to EC_RSTBTN_N signal. Low Active.
GPC42	GPIO Output	EC_SLP_S3_N	EC output to carrier SLP_S3_N signal. This pin will echo CPU_SLP_S3_N status.
GPC43	ADC	EC_ADC0_VCCCPU	EC ADC interface. Used to monitor module PVCCCPU voltage.
GPC44	ADC	EC_ADC1_P3V30A	EC ADC interface. Used to monitor module P3V30A voltage.
GPC45	ADC	EC_ADC2_SVS8	EC ADC interface. Used to monitor carrier output SVS8 voltage.
GPC46	ADC	EC_ADC3_VIN12	EC ADC interface. Used to monitor carrier output VIN12 voltage.
GPC47	ADC	EC_ADC4_VDDQ	EC ADC interface. Used to monitor module VDDQ voltage.
GPC48	GPIO Output	EC_EN_VDDQ	VDDQ power enable signal. Set "High" to enable VDDQ power. Required set EC_EN_SVIDPOWER to "High" before set EC_EN_VDDQ to "High".
GPC49	GPIO Output	EC_EN_PIV80A	PIV80A power enable signal. Set "High" to enable PIV80A power.
GPC50	GPIO Input	VR_PG_PIV80A	PIV80A power good signal. "High" indicating PIV80A power is ready.
GPC51	GPIO Output	EC_BIOS_SPI_MUX_SEL	CPU BIOS SPI Flash select. Set "Low" to select module SPI flash. Set "High" to select carrier SPI flash.
GPC52	GPIO Output	EC_BIOS_SPI_MUX_EN_N	Enable/Disable CPU access SPI flash. Set "Low" to enable CPU access SPI flash.
GPC53	GPIO Output	EC_SPI_MUX_SEL	Enable/Disable EC access BIOS SPI flash. Set "High" to let EC access BIOS SPI flash (it is required to config SSPI pin to SPI function).
GPC54	GPIO Output	EC_I218_DISABLE_N	I218 DISABLE_N signal. Set "Low" to disable I218.
GPC55	GPIO Input	VR_PG_VDDQ	VDDQ power good signal. "High" indicating VDDQ power is ready.
GPC56	GPIO Output	EC_EN_SVIDPOWER	SVID power enable signal. It is required to set EC_EN_SVIDPOWER "High" before enable PVCCCPU, PVCCRAM, PVNN or VDDQ.
GPC57	N/A	GND	Reserved.
GPC58	N/A	EC_CK32KE	Reserved.
GPC59	LPC	LPC_EC_LAD0	LPC interface.
GPC60	LPC	LPC_EC_LAD1	LPC interface.
GPC61	LPC	LPC_EC_LAD2	LPC interface.
GPC62	LPC	LPC_EC_LAD3	LPC interface.
GPC63	LPC	LPC_DEVICE_CLKOUT0	LPC interface.
GPC64	LPC	LPC_EC_FRAME_N	LPC interface.
GPC65	LPC	LPC_EC_SERIRQ	LPC interface.
KS10	GPIO Output*	LAN0_PORT0_LED0	H/W default is LED000 display output. Set "High" to turn on LED. Required EC_LED_PWR_EN to set "High". Alternative function is CPU I0G LED output to EC.
KS11	GPIO Output*	LAN0_PORT0_LED1	H/W default is LED001 display output. Set "High" to turn on LED. Required EC_LED_PWR_EN to set "High". Alternative function is CPU I0G LED output to EC.
KS12	GPIO Output*	LAN0_PORT1_LED0	H/W default is LED010 display output. Set "High" to turn on LED. Required EC_LED_PWR_EN to set "High". Alternative function is CPU I0G LED output to EC.
KS13	GPIO Output*	LAN0_PORT1_LED1	H/W default is LED011 display output. Set "High" to turn on LED. Required EC_LED_PWR_EN to set "High". Alternative function is CPU I0G LED output to EC.
KS14	GPIO Output*	LAN1_PORT0_LED0	H/W default is LED100 display output. Set "High" to turn on LED. Required EC_LED_PWR_EN to set "High". Alternative function is CPU I0G LED output to EC.
KS15	GPIO Output*	LAN1_PORT0_LED1	H/W default is LED101 display output. Set "High" to turn on LED. Required EC_LED_PWR_EN to set "High". Alternative function is CPU I0G LED output to EC.
KS16	GPIO Output*	LAN1_PORT1_LED0	H/W default is LED110 display output. Set "High" to turn on LED. Required EC_LED_PWR_EN to set "High". Alternative function is CPU I0G LED output to EC.
KS17	GPIO Output*	LAN1_PORT1_LED1	H/W default is LED111 display output. Set "High" to turn on LED. Required EC_LED_PWR_EN to set "High". Alternative function is CPU I0G LED output to EC.
KS00	GPIO Input	COME_GP10	Carrier output to EC GP10 signal.
KS01	GPIO Input	COME_GP11	Carrier output to EC GP11 signal.
KS02	GPIO Input	COME_GP12	Carrier output to EC GP12 signal.
KS03	GPIO Input	COME_GP13	Carrier output to EC GP13 signal.
KS04	GPIO Output	EC2COME_GP00	EC output to carrier GP00 signal.
KS05	GPIO Output	EC2COME_GP01	EC output to carrier GP01 signal.
KS06	GPIO Output	EC2COME_GP02	EC output to carrier GP02 signal.
KS07	GPIO Output	EC2COME_GP03	EC output to carrier GP03 signal.
KS08	GPIO Input	COME_BATLOW_N	Carrier output to EC BATLOW_N signal. Active Low.
KS09	GPIO Output	EC_LPC_EN	Enable LPC clock buffer and SERIRQ interface. Set "High" to enable LPC clock output to TPM and carrier, and also enable CPU SERIRQ access.
KS100	GPIO Output	EC_USB_EN	Enable CPU USB2.0 connect to carrier. Set "High" to enable connection.
KS101	GPIO Output	EC_EN_CPU_SMB_LEG	Enable CPU SMB_LEG and DDR SMB access. Set "High" to enable connection.
KS102	GPIO Output	EC_EN_CPU_SMB_HOST	Enable CPU SMB_HOST access. Set "High" to enable connection.
KS103	GPIO Output	EC_EN_CPU_SMB_PECI	Enable CPU SMB_PECI access. Set "High" to enable connection.
KS104	GPIO Output	COME_WDT	EC output to carrier WDT signal.
KS105	GPIO Input	VR_SVIDPOWER_OVP_N	SVID Power OVP indication. "Low" indicating there is an OVP event at SVID power group.

Pin	Alt. Function	Net Name	Description
GPA6	SPI*	SPI_EC_SSCK	EC SSPI interface. Required EC_BIOS_SPI_MUX_SEL, EC_BIOS_SPI_MUX_EN_N and EC_SPI_MUX_SEL to be config properly.
GPC3	SPI*	SPI_EC_SMOSI	EC SSPI interface. Required EC_BIOS_SPI_MUX_SEL, EC_BIOS_SPI_MUX_EN_N and EC_SPI_MUX_SEL to be config properly.
GPC5	SPI*	SPI_EC_SMISO	EC SSPI interface. Required EC_BIOS_SPI_MUX_SEL, EC_BIOS_SPI_MUX_EN_N and EC_SPI_MUX_SEL to be config properly.
GPC11	SPI*	I2C_EC_CLK_SER1_N	EC SMB interface. Used to access I0G LED control device at carrier board (eg. PCA9539). H/W Default is connected to SER1
GPA1	SMBUS*	I2C_EC_CLK_SER1_RX	EC SMB interface. Used to access I0G LED control device at carrier board (eg. PCA9539). H/W Default is connected to SER1
GPC2	SMBUS*	I2C_EC_DAT_SER1_TX	CPU output to EC I0G interface LED (LAN0, Port0, LED0). H/W default is LED000 display output.
KS10	GPIO Input*	LAN0_PORT0_LED0	CPU output to EC I0G interface LED (LAN0, Port0, LED0). H/W default is LED000 display output.
KS11	GPIO Input*	LAN0_PORT0_LED1	CPU output to EC I0G interface LED (LAN0, Port0, LED0). H/W default is LED001 display output.
KS12	GPIO Input*	LAN0_PORT1_LED0	CPU output to EC I0G interface LED (LAN0, Port1, LED0). H/W default is LED010 display output.
KS13	GPIO Input*	LAN0_PORT1_LED1	CPU output to EC I0G interface LED (LAN0, Port1, LED1). H/W default is LED011 display output.
KS14	GPIO Input*	LAN1_PORT0_LED0	CPU output to EC I0G interface LED (LAN1, Port0, LED0). H/W default is LED100 display output.
KS15	GPIO Input*	LAN1_PORT0_LED1	CPU output to EC I0G interface LED (LAN1, Port0, LED1). H/W default is LED101 display output.
KS16	GPIO Input*	LAN1_PORT1_LED0	CPU output to EC I0G interface LED (LAN1, Port1, LED0). H/W default is LED110 display output.
KS17	GPIO Input*	LAN1_PORT1_LED1	CPU output to EC I0G interface LED (LAN1, Port1, LED1). H/W default is LED111 display output.

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CPU Hardware Strap

Pin	Net Name	Strap Name	Int. Connection	Ext. Connection	Setting
BR58	CPU_STRAP_ERROR_N1	Boot BIOS Strap	20K PD	10k PD	0 = SPI
BL52	CPU_STRAP_ERROR_N0	LPC Decode Select	20K PD	10k PD	0 = Low Pin Count (LPC)
BN52	MCERR_N	Reserved for Intel	20k PD	No Connection	Reserved
BW50	CPU_STRAP_IERR_N	Flash Security Override	20k PD	10k PD	0 = Flash descriptor security locked
BN56	CPU_STRAP_TCO_Reboot_Enable	No TCO Reboot Enable	20k PD	1k PU	1 = Stop the TCO watchdog timer from rebooting the system after the second timeout.
BN44	CPU_STRAP_Top_Swap_Override	Top Swap Override	20k PD	10k PD	0 = Top-swap feature is disabled.
BE44	CPU_STRAP_ME_RCVR_N	Forces ME into Recovery Mode	20k PU	1k PU	1 = Normal operating mode for Intel ME.
BY58	CPU_STRAP_RSVD_BY58	Reserved for Intel	20K PU	10k PU	Reserved
CA50	CPU_STRAP_ERROR_N2	Reserved for Intel	20K PD	No Connection	Reserved
BA69	LAN1_PORT1_I2C_CLK_STRAP	Reserved for Intel	20K PU	10k PU	Reserved
W58	LAN1_PORT1_I2C_DATA_STRAP	Reserved for Intel	20K PU	10k PU	Reserved
BF70	CPU_STRAP_Reserved_BF70	Reserved for Intel	20K PU	No Connection	Reserved
BK69	LAN_MDC_STRAP	Reserved for Intel	20K PU	4.7k PU	Reserved
BK71	LAN_MDIO_STRAP	Reserved for Intel	20K PU	4.7k PU	Reserved
BU57	CPU_STRAP_SATA0_SDOUT	Reserved for Intel	20K PU	No Connection	Reserved
BN66	SMB_CPU_LAN_ALERT_N_STRAP	Reserved for Intel	20K PU	4.7k PU	Reserved
BV58	CPU_SUS_STAT_N_STRAP	Reserved for Intel	20K PU	10k PU	Reserved
BG48	CPU_STRAP_FLEX_CLK_SE0	Reserved for Intel	20K PD	No Connection	Reserved
CA48	CPU_STRAP_FLEX_CLK_SE1	Reserved for Intel	20K PU	No Connection	Reserved
CA52	UART0_CPU_TXD_STRAP	Reserved for Intel	20K PD	No Connection	Reserved
BN59	UART1_CPU_TXD_STRAP	Reserved for Intel	20K PU	No Connection	Reserved

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A	11_CPU_Hardware_Strap		
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CPU HSIO Configuration

HSIO Lane #	Interface
HSIO Lane 0	PCIe 3.0 x8 (Root Port 0)
HSIO Lane 1	PCIe 3.0 x8 (Root Port 0)
HSIO Lane 2	PCIe 3.0 x8 (Root Port 0)
HSIO Lane 3	PCIe 3.0 x8 (Root Port 0)
HSIO Lane 4	PCIe 3.0 x8 (Root Port 0)
HSIO Lane 5	PCIe 3.0 x8 (Root Port 0)
HSIO Lane 6	PCIe 3.0 x8 (Root Port 0)
HSIO Lane 7	PCIe 3.0 x8 (Root Port 0)
HSIO Lane 8	PCIe 3.0 x2 (Root Port 4)
HSIO Lane 9	PCIe 3.0 x2 (Root Port 4)
HSIO Lane 10	PCIe 3.0 x1 (Root Port 5)
HSIO Lane 11	SATA 3.0 Controller 0 Port 7 (Unused)
HSIO Lane 12	PCIe 3.0 x2 (Root Port 6)
HSIO Lane 13	PCIe 3.0 x2 (Root Port 6)
HSIO Lane 14	SATA 3.0 Controller 1 Port 2
HSIO Lane 15	SATA 3.0 Controller 1 Port 3
HSIO Lane 16	USB 3.0 Port 1 (USB port 0)
HSIO Lane 17	USB 3.0 Port 2 (USB port 1)
HSIO Lane 18	USB 3.0 Port 3 (USB port 2) (Unused)
HSIO Lane 19	USB 3.0 Port 4 (USB port 3) (Unused)

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A	12_CPU_HSIO_Configuration	

XDP Pin Define

Pin	Signal Name	Pin	Signal Name
1	P1V05A	2	TMS
3	TCK	4	TDO
5	TDI	6	RSTBTN_N
7	PLTRST_N	8	10k ohm to GND
9	TRST_N	10	CX_PREQ_N
11	CX_PRDY_N	12	P1V05A
13	DFX_PORT_CLK0	14	No Connect
15	UART1_TXD_STRAP	16	GND
17	GND	18	No Connect
19	DFX_PORT0	20	No Connect
21	DFX_PORT1	22	No Connect
23	DFX_PORT2	24	No Connect
25	DFX_PORT3	26	No Connect
27	DFX_PORT4	28	No Connect
29	DFX_PORT5	30	No Connect
31	DFX_PORT6	32	No Connect
33	DFX_PORT7	34	RSTBTN_N
35	DFX_PORT8	36	SUS_STAT_N_STRAP
37	DFX_PORT9	38	PLTRST_N
39	DFX_PORT10	40	PWRBTN_N
41	DFX_PORT11	42	RSMRST_N
43	DFX_PORT12	44	Reserved
45	DFX_PORT13	46	Reserved
47	DFX_PORT14	48	I2C_SCL
49	DFX_PORT15	50	I2C_SDA
51	No Connect	52	No Connect
53	No Connect	54	UART0_TXD
55	No Connect	56	UART0_RXD
57	GND	58	GND
59	DFX_PORT_CLK1	60	No Connect

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COMe Reserved Pin

Pin	Module Reserved	Signal	Description
A29	PCIE_CLKOUT1_DP		CPU output PCIe reference clock positive signal of differential pair 1.
A30	PCIE_CLKOUT1_DN		CPU output PCIe reference clock negative signal of differential pair 1.
A32	PCIE_CLKOUT2_DP		CPU output PCIe reference clock positive signal of differential pair 2.
A33	PCIE_CLKOUT2_DN		CPU output PCIe reference clock negative signal of differential pair 2.
A48	PCIE_CLKREQ1_N		CPU PCIe clock request signal 1. Active Low.
A86	PCIE_CLKREQ2_N		CPU PCIe clock request signal 2. Active Low.
A87	PCIE_CLKREQ3_N		CPU PCIe clock request signal 3. Active Low.
B28	GND		Module connect to GND for better return path of differential signal.
B29	PCIE_CLKOUT3_DP		CPU output PCIe reference clock positive signal of differential pair 3.
B30	PCIE_CLKOUT3_DN		CPU output PCIe reference clock negative signal of differential pair 3.
C63	LAN0_PORT0_LED0		CPU 10G LAN 0 port 0 LED 0 signal. Active Low.
C64	LAN0_PORT0_LED1		CPU 10G LAN 0 port 0 LED 1 signal. Active Low.
C77	LAN1_PORT0_LED0		CPU 10G LAN 1 port 0 LED 0 signal. Active Low.
C83	LAN1_PORT1_LED0		CPU 10G LAN 1 port 1 LED 0 signal. Active Low.
C97	N/A		N/A
D36	N/A		N/A
D37	N/A		N/A
D54	N/A		N/A
D63	LAN0_PORT1_LED0		CPU 10G LAN 0 port 1 LED 0 signal. Active Low.
D64	LAN0_PORT1_LED1		CPU 10G LAN 0 port 1 LED 1 signal. Active Low.
D77	LAN1_PORT0_LED1		CPU 10G LAN 1 port 0 LED 1 signal. Active Low.
D83	LAN1_PORT1_LED1		CPU 10G LAN 1 port 1 LED 1 signal. Active Low.
D97	N/A		N/A

Note: All COMe reserved pins signal default are not applied.

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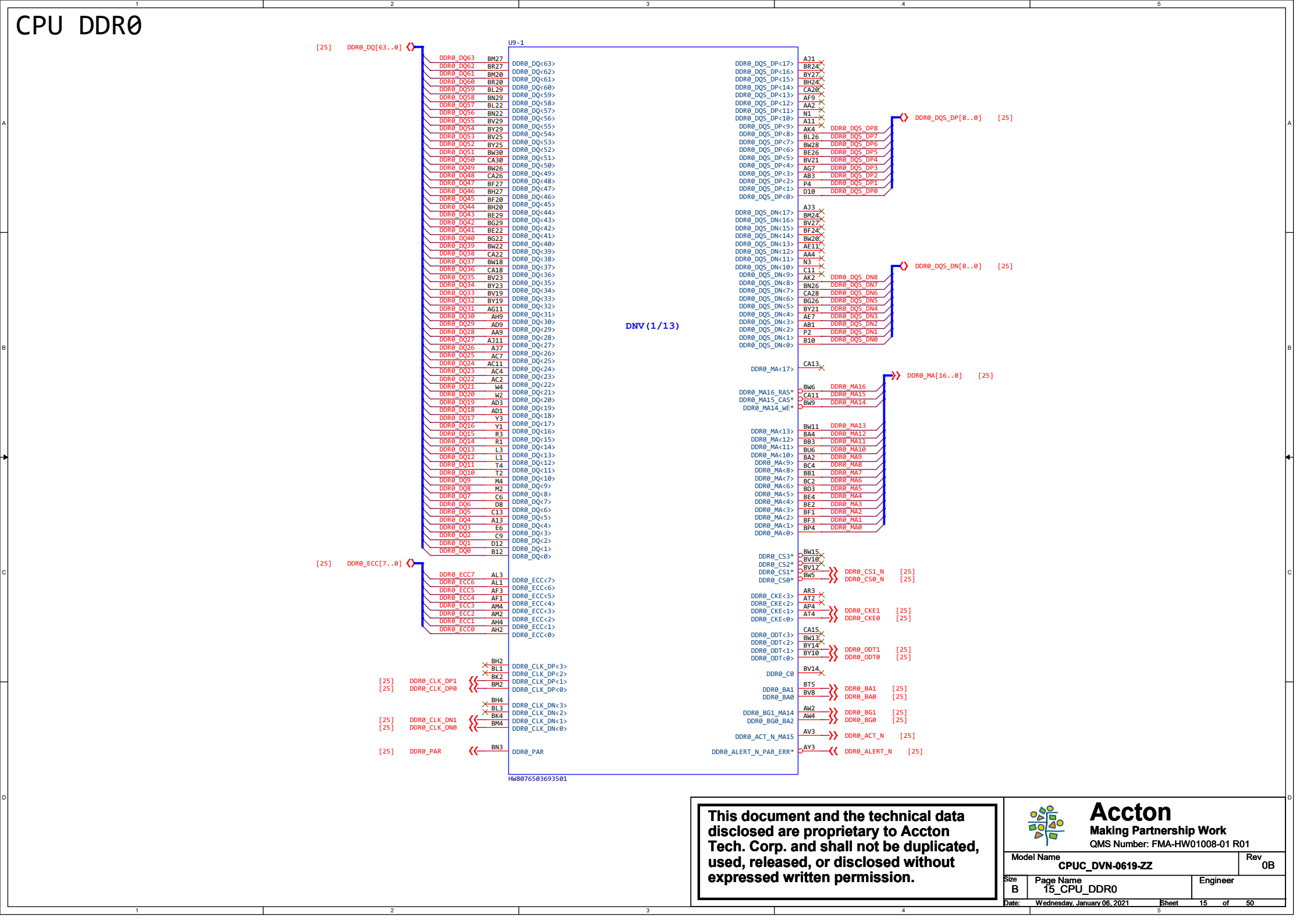


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[illegible][illegible][illegible][illegible][illegible]

CPU DDR0

[25] DDR0_DQ[63..0]

U9-1

DDR0_DQ<63> BM27
DDR0_DQ<62> BR27
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DDR0_MA<4>
DDR0_MA<3>
DDR0_MA<2>
DDR0_MA<1>
DDR0_MA<0>

DDR0_CS3* BW15
DDR0_CS2* BV10
DDR0_CS1* BV12
DDR0_CS0* BW5

DDR0_CS1_N [25]
DDR0_CS0_N [25]

AR3
AT2
AP4
AT4

DDR0_CKE<3>
DDR0_CKE<2>
DDR0_CKE<1>
DDR0_CKE<0>

CA15
BW13
BY14
BV10

DDR0_ODT<3>
DDR0_ODT<2>
DDR0_ODT<1>
DDR0_ODT<0>

BV14

DDR0_C0
BT5
BV8

DDR0_BA1 [25]
DDR0_BA0 [25]

AW2
AW4

DDR0_BG1_MA14 [25]
DDR0_BG0_BA2 [25]

AV3
AY3

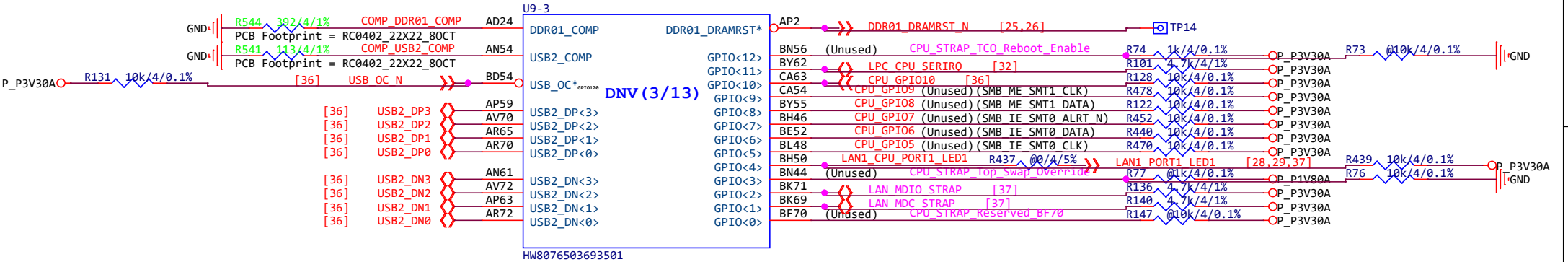
DDR0_ACT_N [25]
DDR0_ALERT_N [25]

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HW8076503693501

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CPU USB



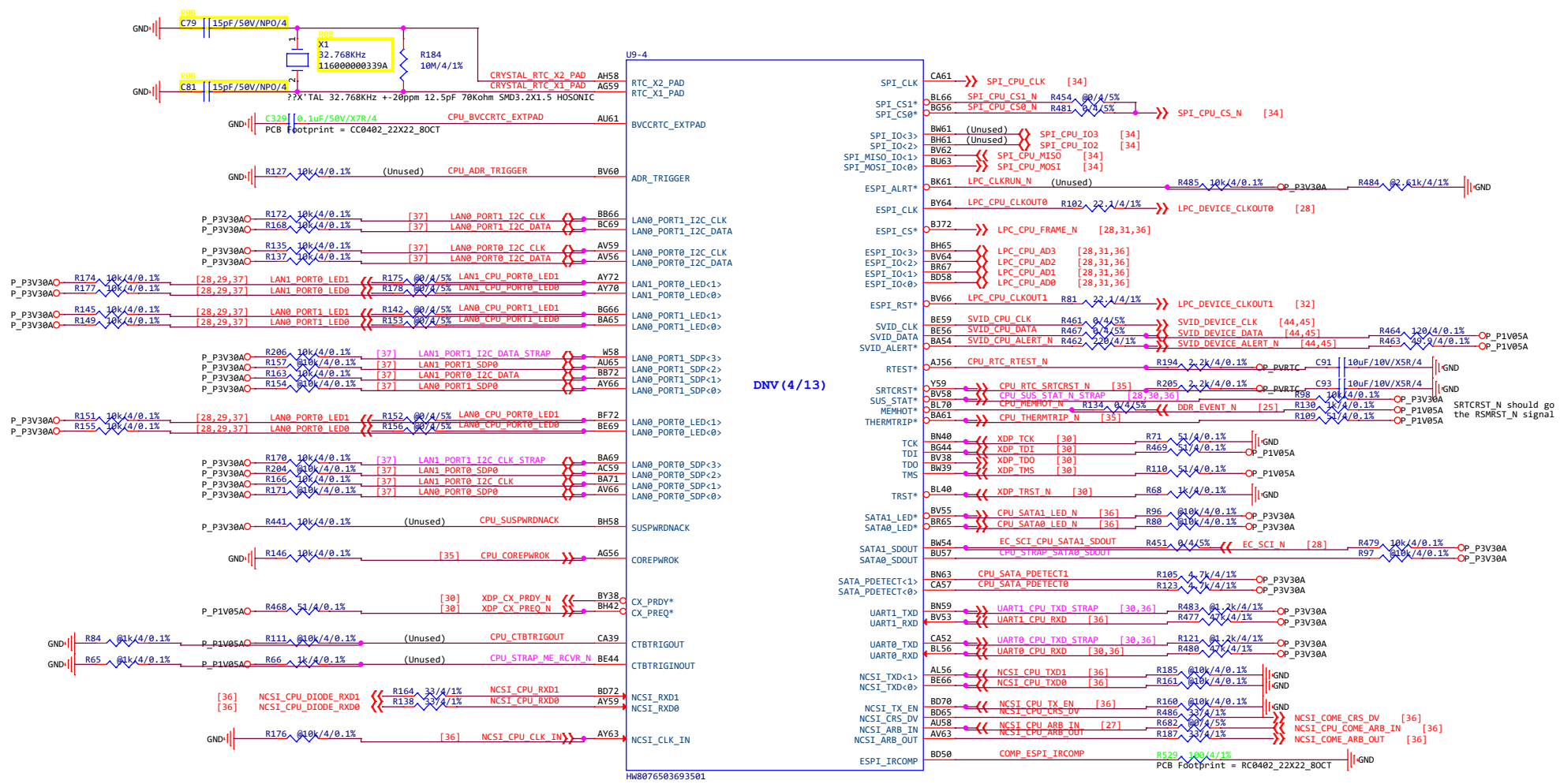
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QMS Number: FMA-HW01008-01 R01

Model Name		Rev
CPUC_DVN-0619-ZZ		0B
Size	Page Name	Engineer
A	17_CPU_USB	
Date:	Wednesday, January 06, 2021	Sheet 17 of 50

CPU LAN LPC SPI NCSI JTAG UART



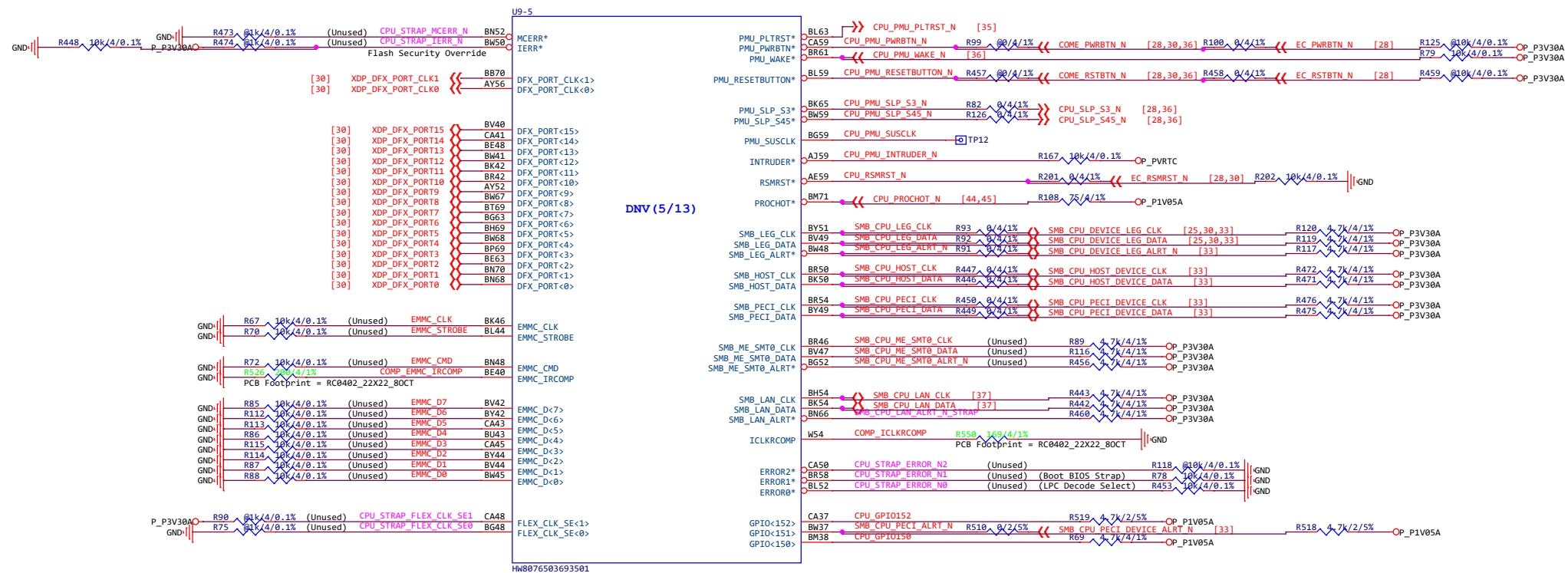
DNV (4/13)

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QMS Number: FMA-HW01008-01 R01

Model Name CPUC_DVN-0619-ZZ		Rev 0B
Size B	Page Name 18_CPU_LPC_SPI_NCSI_JTAG_UART	Engineer
Date: Wednesday, January 06, 2021	Sheet 18	of 50



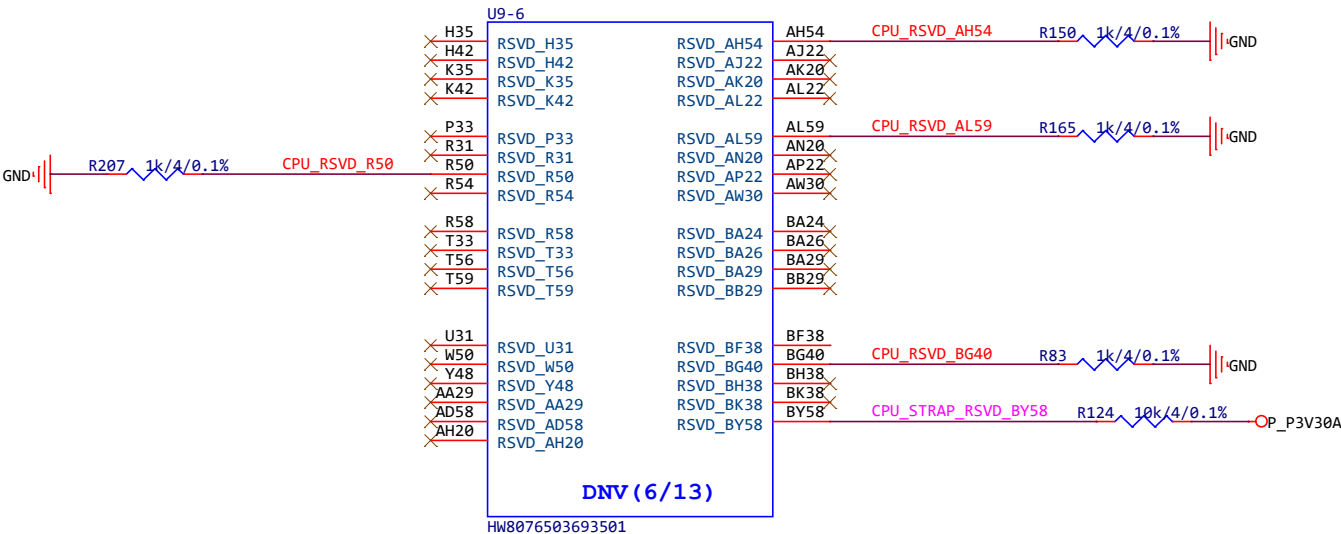
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QMS Number: FMA-HW01008-01 R01

Model Name CPUC_DVN-0619-ZZ		Rev 0B
Size B	Page Name 19_CPU_PMU_SMB	Engineer
Date: Wednesday, January 06, 2021		Sheet 19 of 50

CPU RSVD



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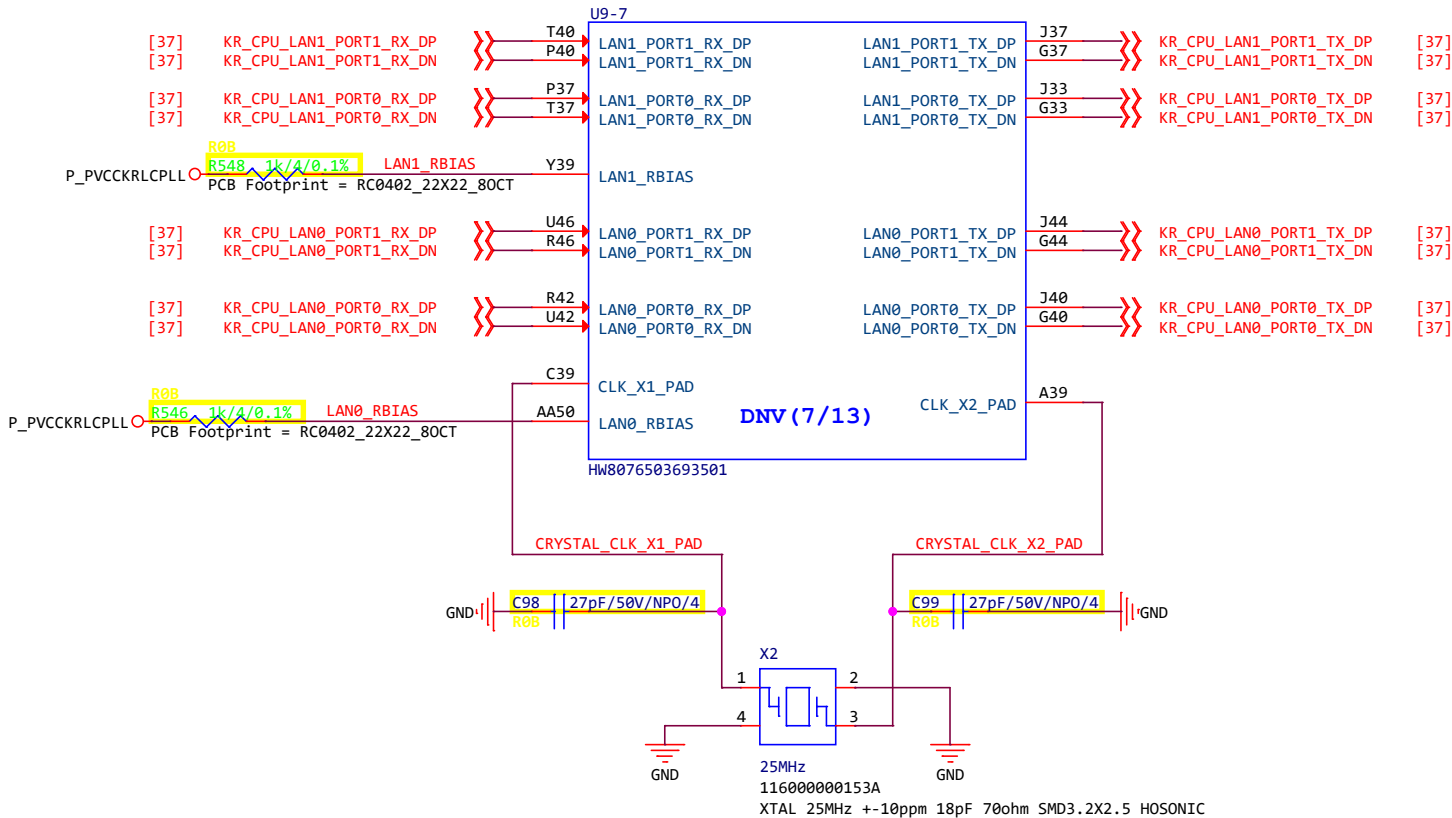
QMS Number: FMA-HW01008-01 R01

Model Name	CPUC_DVN-0619-ZZ	Rev	0B
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Size	Page Name	Engineer
A	20_CPU_RSVD	

Date:	Wednesday, January 06, 2021	Sheet	20	of	50
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CPU KR



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QMS Number: FMA-HW01008-01 R01

Model Name		Rev
CPUC_DVN-0619-ZZ		0B
Size	Page Name	Engineer
A	21_CPU_KR	
Date:	Wednesday, January 06, 2021	Sheet 21 of 50

CPU Power

Bill of Materials Table:

Part	Value	Qty
VDDQ	0.1uF/16V/X7R/4	x1
	1uF/10V/X5R/4	x2
PVCCCPU	10uF/6.3V/X5R/4	x5
	1uF/10V/X5R/4	x8
	1uF/6.3V/X5R/2	x6
PVCCRAM	1uF/6.3V/X5R/2	x1
	2.2uF/6.3V/X5R/4	x2
PVNN	22uF/6.3V/X5R/4	x2
	4.7uF/6.3V/X5R/2	x6
PVCCREF_P1V24	10uF/6.3V/X5R/6	x1
P1V05A	22uF/6.3V/X5R/4	x10
	4.7uF/6.3V/X5R/2	x5
P1V80A	10uF/6.3V/X5R/4	x1
	1uF/10V/X5R/4	x1
	1uF/6.3V/X5R/2	x1
P3V30A	10uF/6.3V/X5R/4	x1

Place under CPU (bottom layer)

Bill of Materials Table:

Part	Value	Qty
VDDQ	0.1uF/16V/X7R/4	x1
	1uF/10V/X5R/4	x2
PVCCCPU	10uF/6.3V/X5R/4	x5
	1uF/10V/X5R/4	x8
	1uF/6.3V/X5R/2	x6
PVCCRAM	1uF/6.3V/X5R/2	x1
	2.2uF/6.3V/X5R/4	x2
PVNN	22uF/6.3V/X5R/4	x2
	4.7uF/6.3V/X5R/2	x6
PVCCREF_P1V24	10uF/6.3V/X5R/6	x1
P1V05A	22uF/6.3V/X5R/4	x10
	4.7uF/6.3V/X5R/2	x5
P1V80A	10uF/6.3V/X5R/4	x1
	1uF/10V/X5R/4	x1
	1uF/6.3V/X5R/2	x1
P3V30A	10uF/6.3V/X5R/4	x1

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Model Name		Rev	
CPUC_DVN-0619-ZZ		0B	
Size	Page Name	Engineer	
C	23_CPU_POWER		
Date	Wednesday, January 08, 2021	Sheet	23 of 50

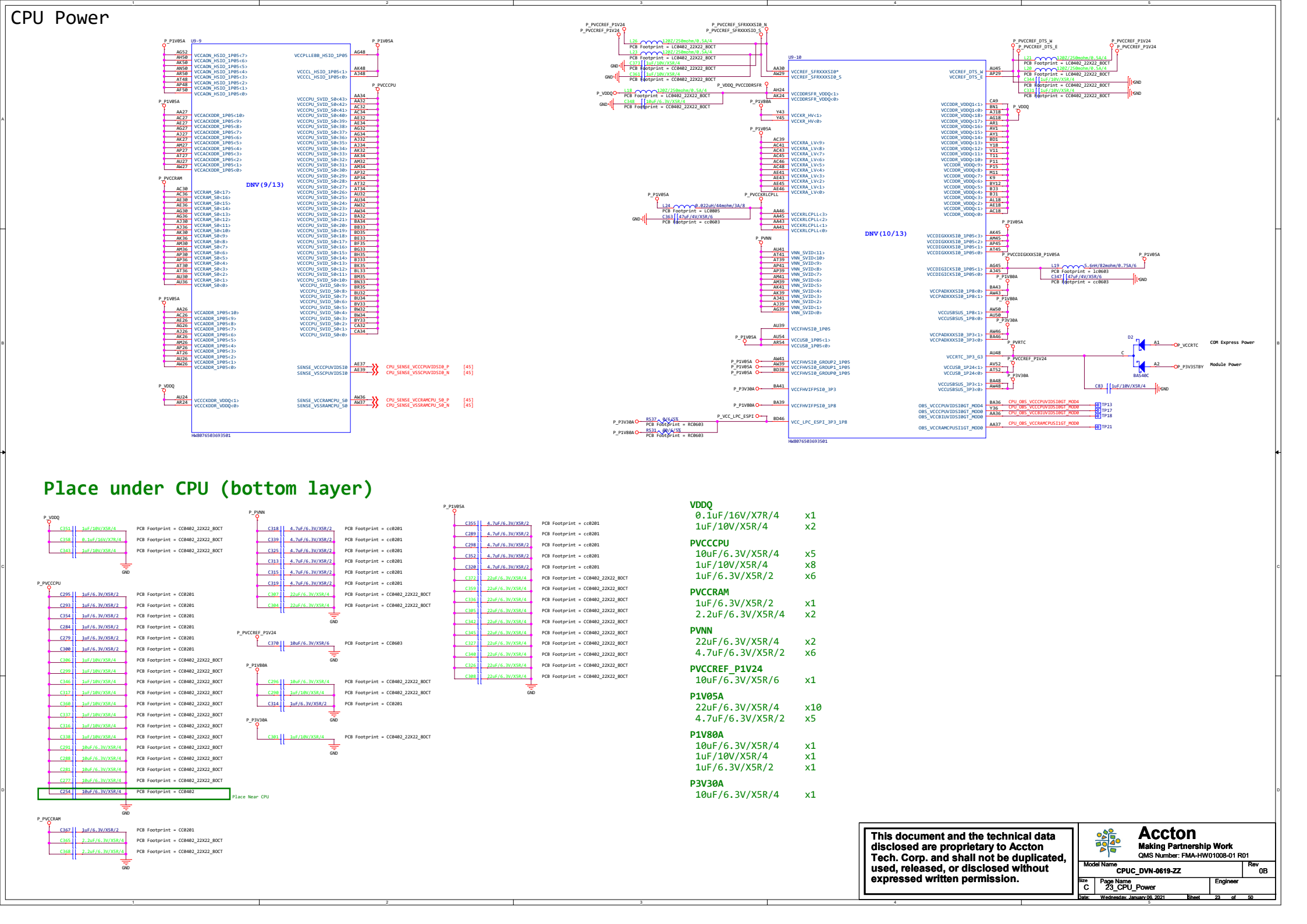
CPU Power

Place under CPU (bottom layer)

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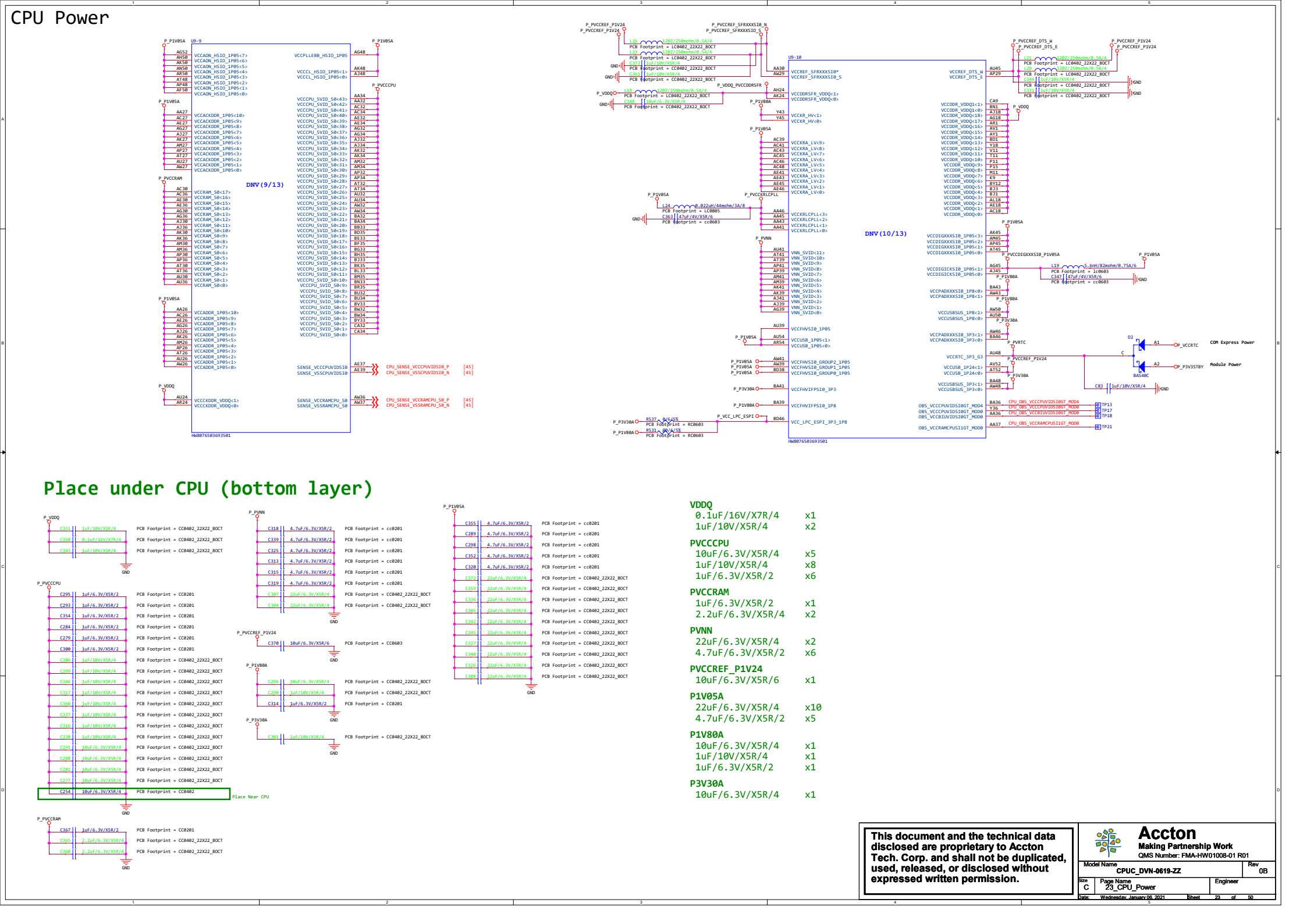
Model Name		Rev	
CPUC_DVN-0619-ZZ		0B	
Size	Page Name	Engineer	
C	23_CPU_POWER		
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CPU Power

Power Plane	Component	Value	Footprint
VCCPLLEB_HSI0_1P05<7>	AC52	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCPLLEB_HSI0_1P05<6>	AC53	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCPLLEB_HSI0_1P05<5>	AC54	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCPLLEB_HSI0_1P05<4>	AC55	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCPLLEB_HSI0_1P05<3>	AC56	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCPLLEB_HSI0_1P05<2>	AC57	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCPLLEB_HSI0_1P05<1>	AC58	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<43>	AC59	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<42>	AC60	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<41>	AC61	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<40>	AC62	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<39>	AC63	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<38>	AC64	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<37>	AC65	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<36>	AC66	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<35>	AC67	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<34>	AC68	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<33>	AC69	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<32>	AC70	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<31>	AC71	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<30>	AC72	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<29>	AC73	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<28>	AC74	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<27>	AC75	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<26>	AC76	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<25>	AC77	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<24>	AC78	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<23>	AC79	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<22>	AC80	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<21>	AC81	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<20>	AC82	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<19>	AC83	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<18>	AC84	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<17>	AC85	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<16>	AC86	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<15>	AC87	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<14>	AC88	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<13>	AC89	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<12>	AC90	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<11>	AC91	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<10>	AC92	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<9>	AC93	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<8>	AC94	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<7>	AC95	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<6>	AC96	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<5>	AC97	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<4>	AC98	100nF/6.3V/X5R/2	CC0802_22X22_B0CT
VCCCPU_VDD<			

CPU Power



CPU Power

Bill of Materials Table:

Part	Value	Footprint	Quantity
VDDQ	0.1uF/16V/X7R/4	x1	
	1uF/10V/X5R/4	x2	
PVCCCPU	10uF/6.3V/X5R/4	x5	
	1uF/10V/X5R/4	x8	
	1uF/6.3V/X5R/2	x6	
PVCCRAM	1uF/6.3V/X5R/2	x1	
	2.2uF/6.3V/X5R/4	x2	
PVNN	22uF/6.3V/X5R/4	x2	
	4.7uF/6.3V/X5R/2	x6	
PVCCREF_P1V24	10uF/6.3V/X5R/6	x1	
P1V05A	22uF/6.3V/X5R/4	x10	
	4.7uF/6.3V/X5R/2	x5	
P1V80A	10uF/6.3V/X5R/4	x1	
	1uF/10V/X5R/4	x1	
	1uF/6.3V/X5R/2	x1	
P3V30A	10uF/6.3V/X5R/4	x1	

Place under CPU (bottom layer)

Bill of Materials Table:

Part	Value	Footprint	Quantity
VDDQ	0.1uF/16V/X7R/4	x1	
	1uF/10V/X5R/4	x2	
PVCCCPU	10uF/6.3V/X5R/4	x5	
	1uF/10V/X5R/4	x8	
	1uF/6.3V/X5R/2	x6	
PVCCRAM	1uF/6.3V/X5R/2	x1	
	2.2uF/6.3V/X5R/4	x2	
PVNN	22uF/6.3V/X5R/4	x2	
	4.7uF/6.3V/X5R/2	x6	
PVCCREF_P1V24	10uF/6.3V/X5R/6	x1	
P1V05A	22uF/6.3V/X5R/4	x10	
	4.7uF/6.3V/X5R/2	x5	
P1V80A	10uF/6.3V/X5R/4	x1	
	1uF/10V/X5R/4	x1	
	1uF/6.3V/X5R/2	x1	
P3V30A	10uF/6.3V/X5R/4	x1	

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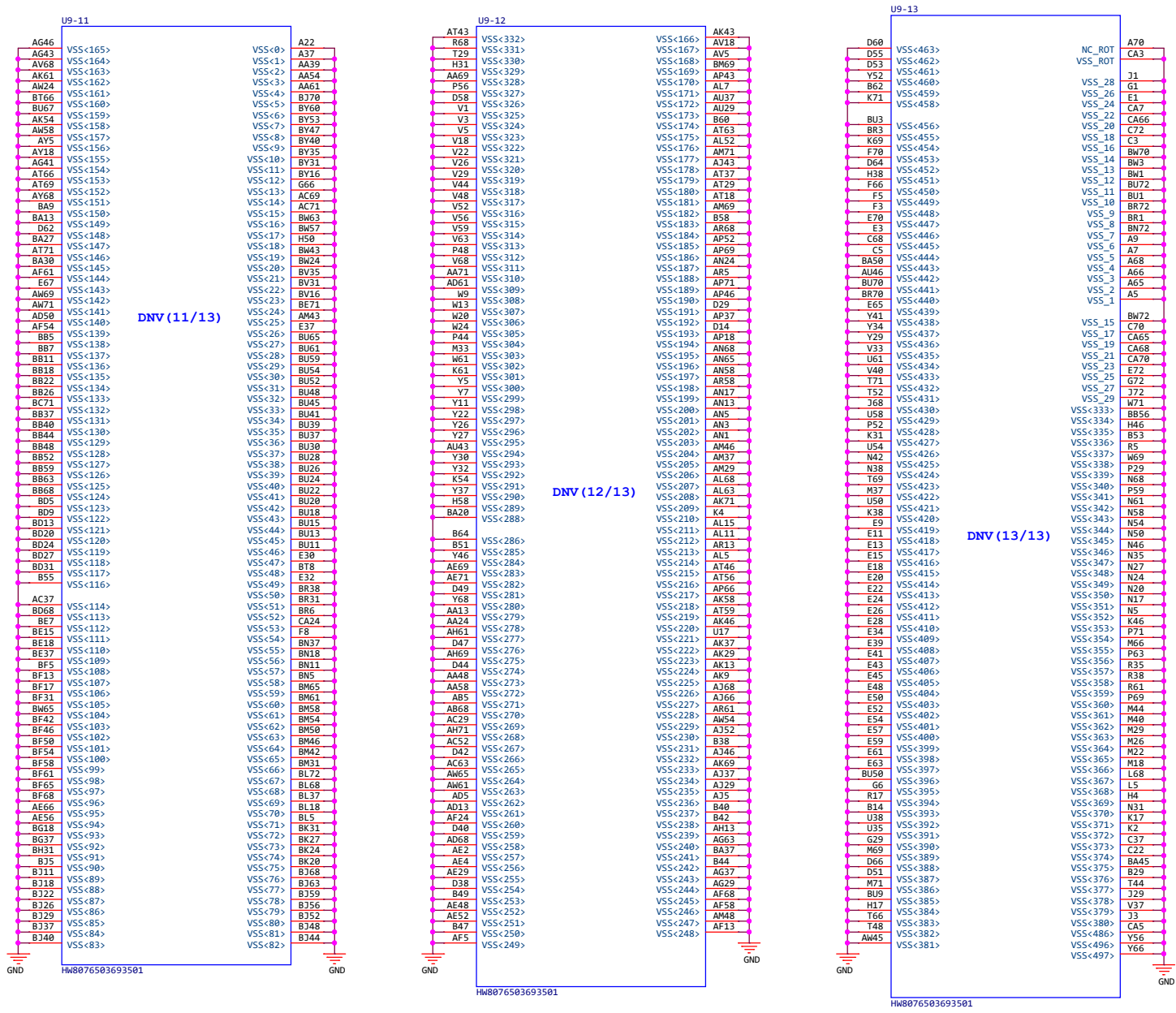
Model Name	Rev
CPUCU-DVN-0619-ZZ	0B

Size	Page Name	Engineer
C	23_CPU_POWER	

Date: Wednesday, January 08, 2021 Sheet: 23 of 50

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CPU GND



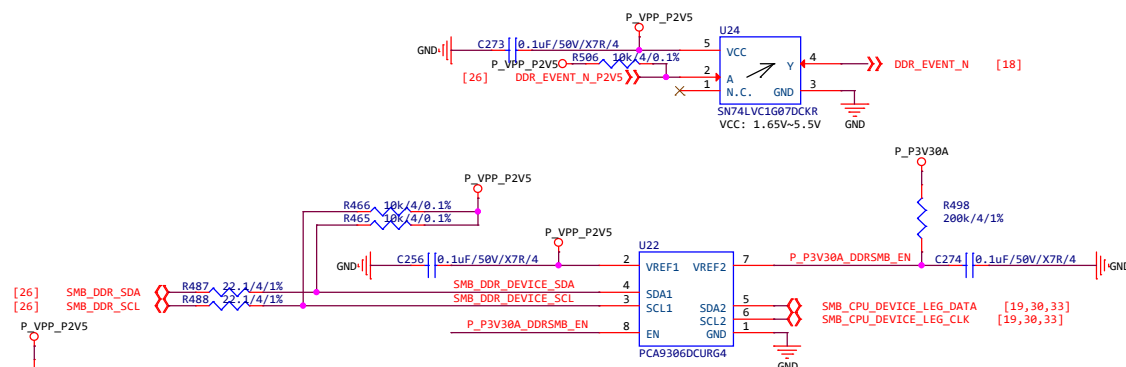
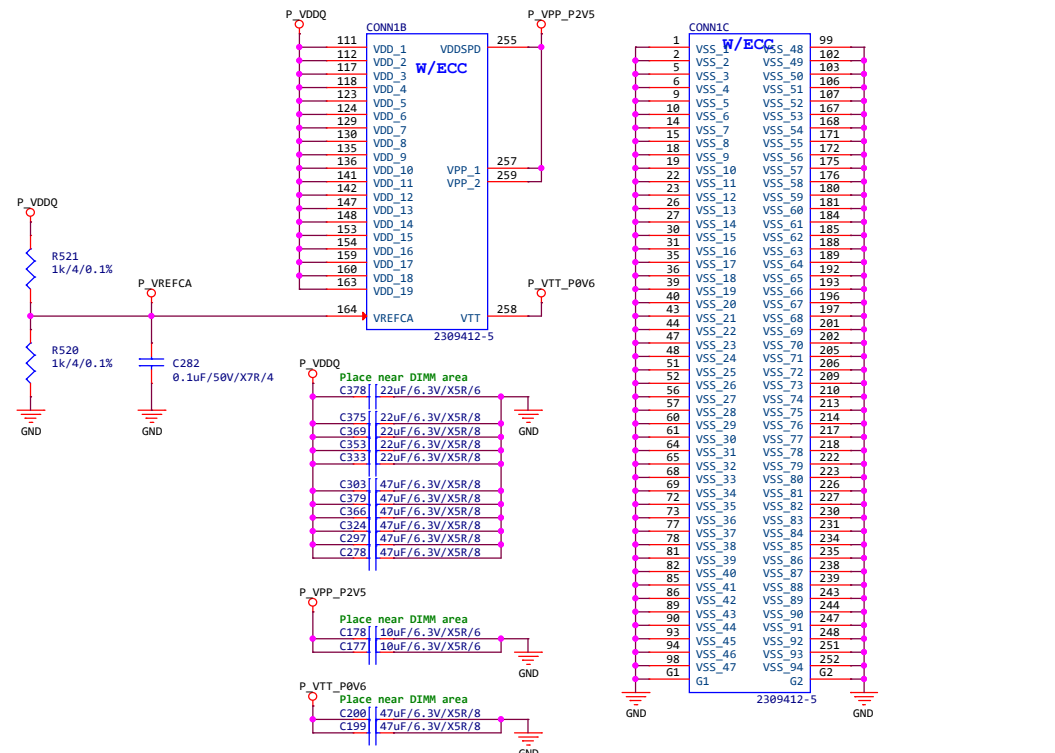
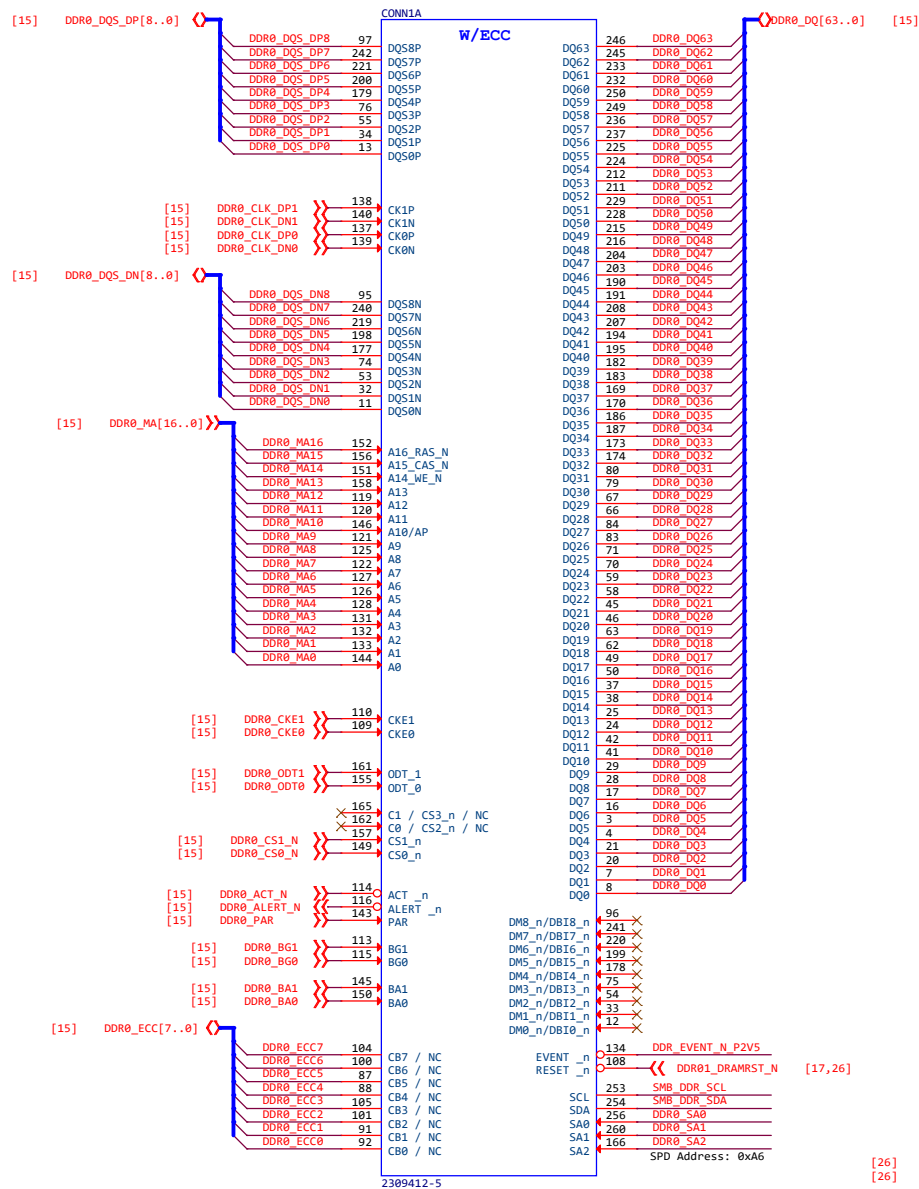
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Model Name CPUC_DVN-0619-ZZ		Rev 0B
Size B	Page Name 24_CPU_GND	Engineer
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DDR0 SODIMM0 8H



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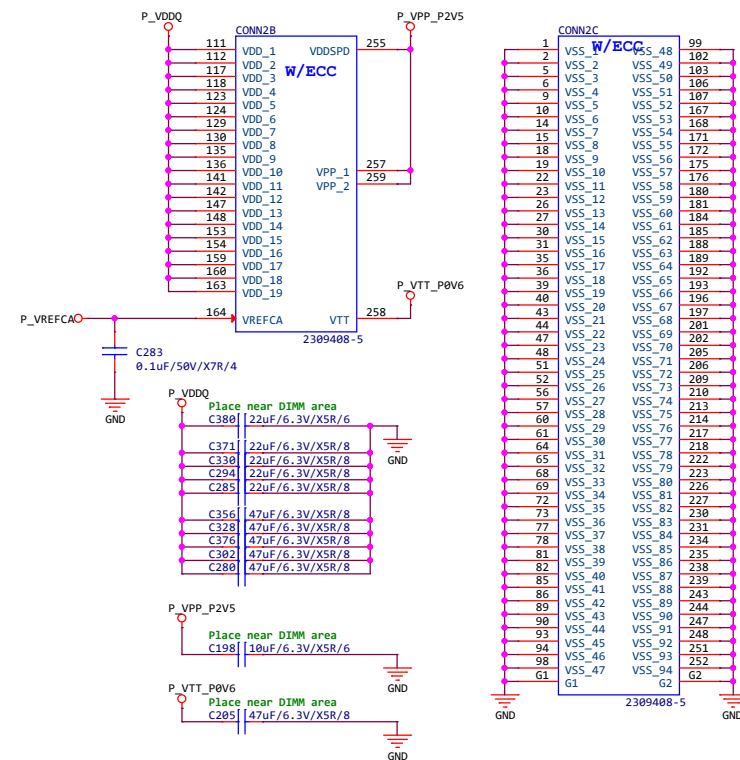
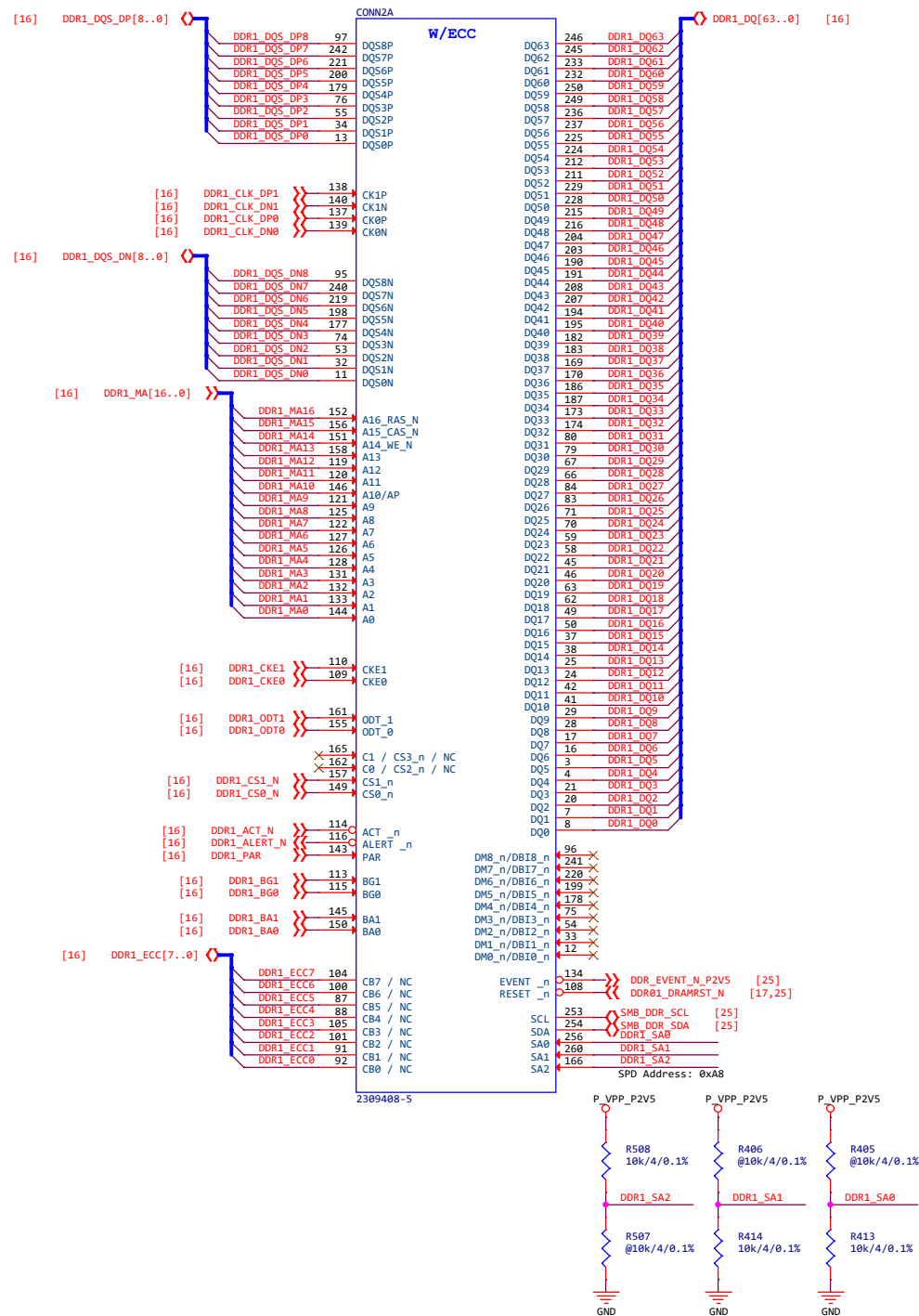
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QMS Number: FMA-HW01008-01 R01

Model Name		Rev
CPUC_DVN-0619-ZZ		0B
Size	Page Name	Engineer
B	25 DDR0 SODIMM 8H	

DDR1 SODIMM0 4H



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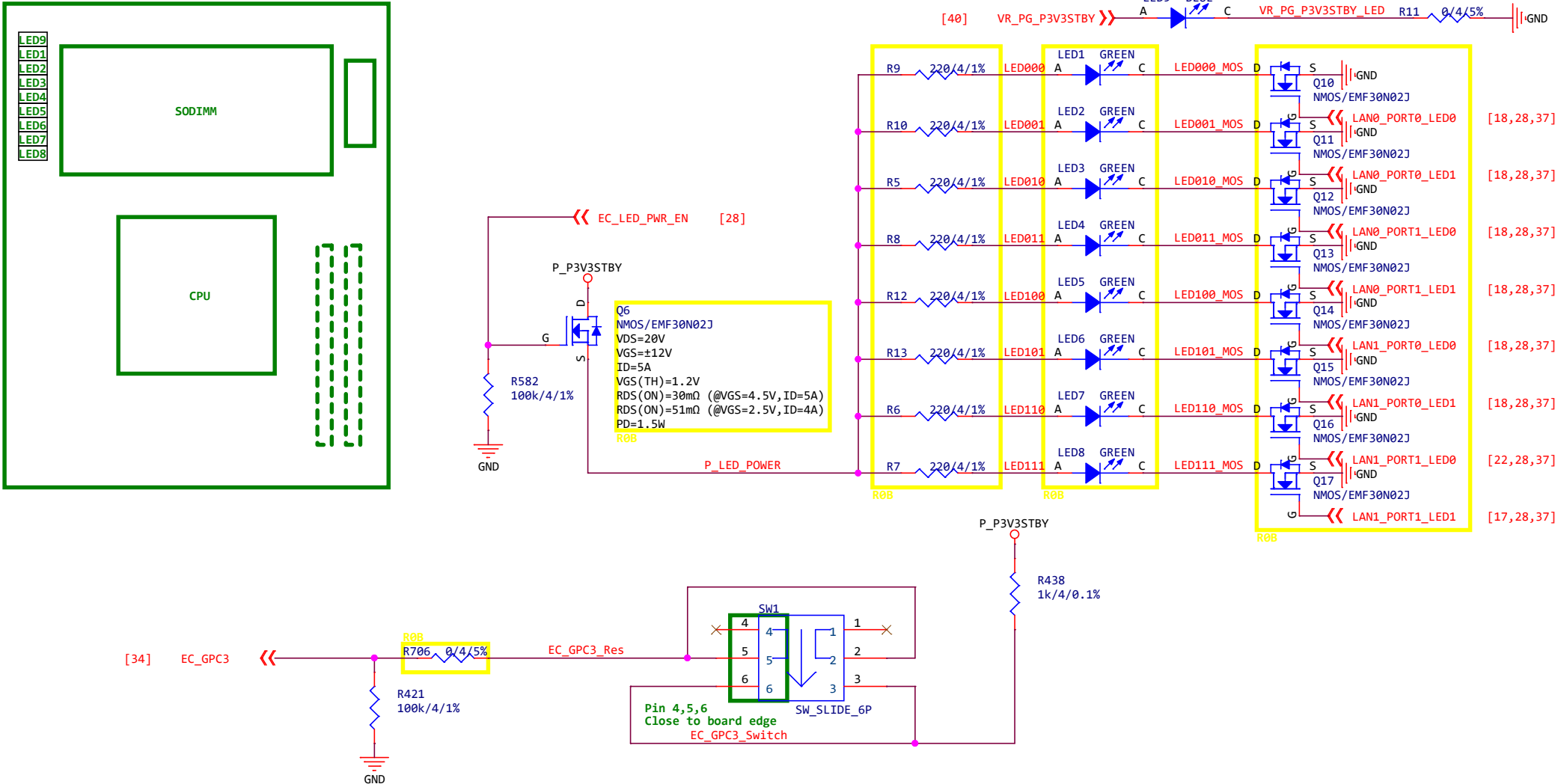
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QMS Number: FMA-HW01008-01 R01

Model Name CPUC_DVN-0619-ZZ		Rev 0B
Size B	Page Name 26_DDR1_SODIMMO_4H	Engineer
Date: Wednesday, January 06, 2021	Sheet	26 of 50

LED and Switch

LED Place at Top Layer



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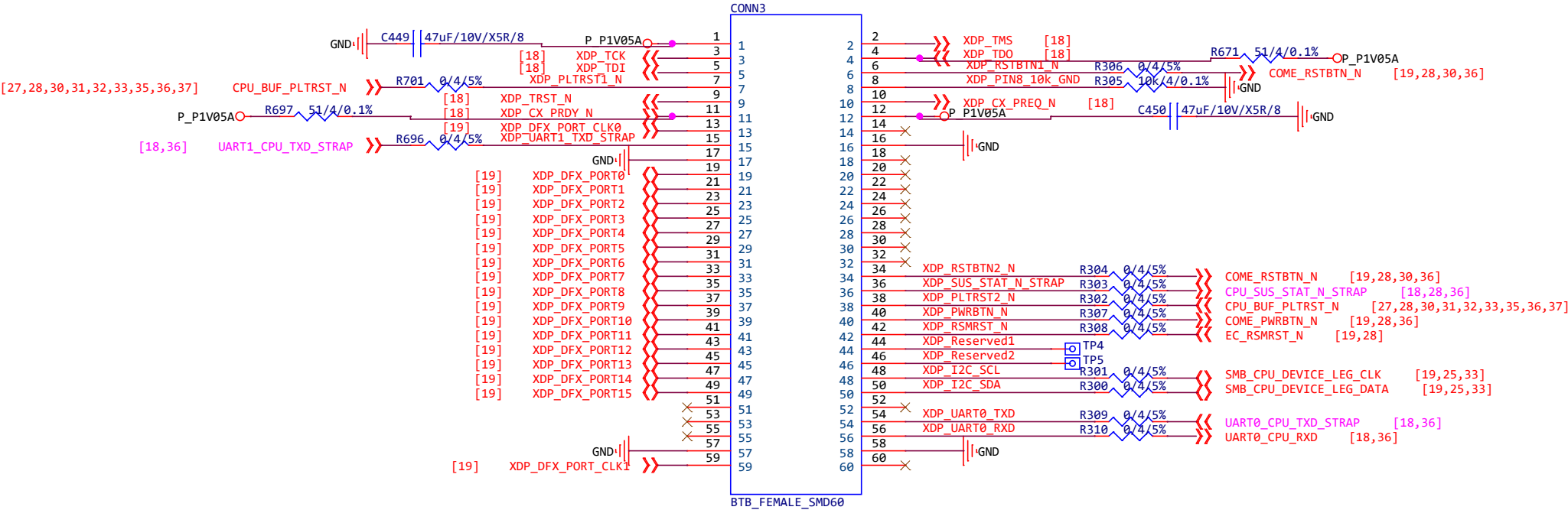
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QMS Number: FMA-HW01008-01 R01

Model Name		Rev
CPUC_DVN-0619-ZZ		0B
Size	Page Name	Engineer
A	29_LED_and_Switch	
Date:	Wednesday, January 06, 2021	Sheet 29 of 50

XDP



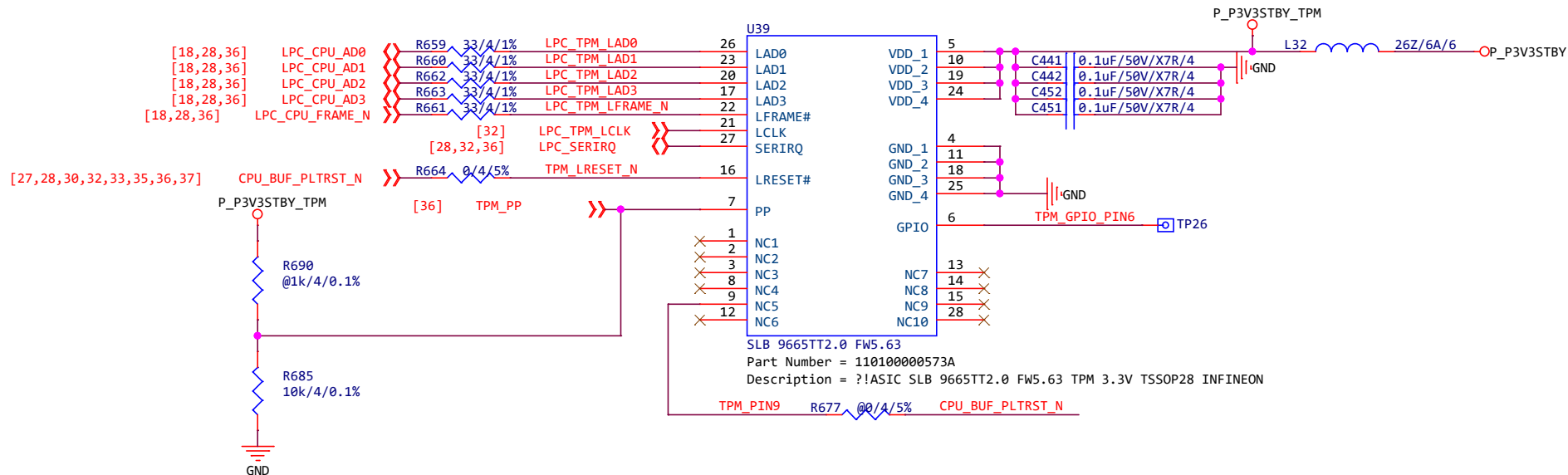
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QMS Number: FMA-HW01008-01 R01

Model Name		Rev
CPUC_DVN-0619-ZZ		0B
Size	Page Name	Engineer
A	30_XDP	
Date:	Wednesday, January 06, 2021	Sheet 30 of 50

TPM



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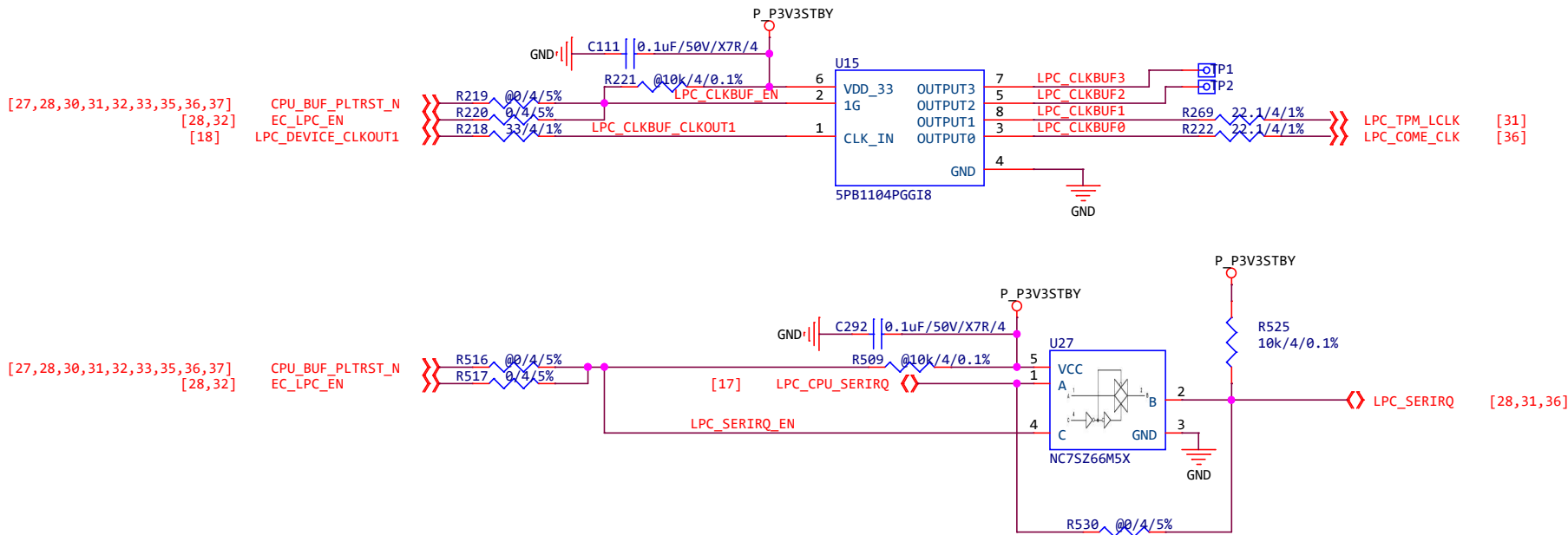
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QMS Number: FMA-HW01008-01 R01

Model Name		Rev	
CPUC_DVN-0619-ZZ		0B	
Size	Page Name	Engineer	
A	31_TPM		
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LPC_CLK_BUFFER SERIRQ



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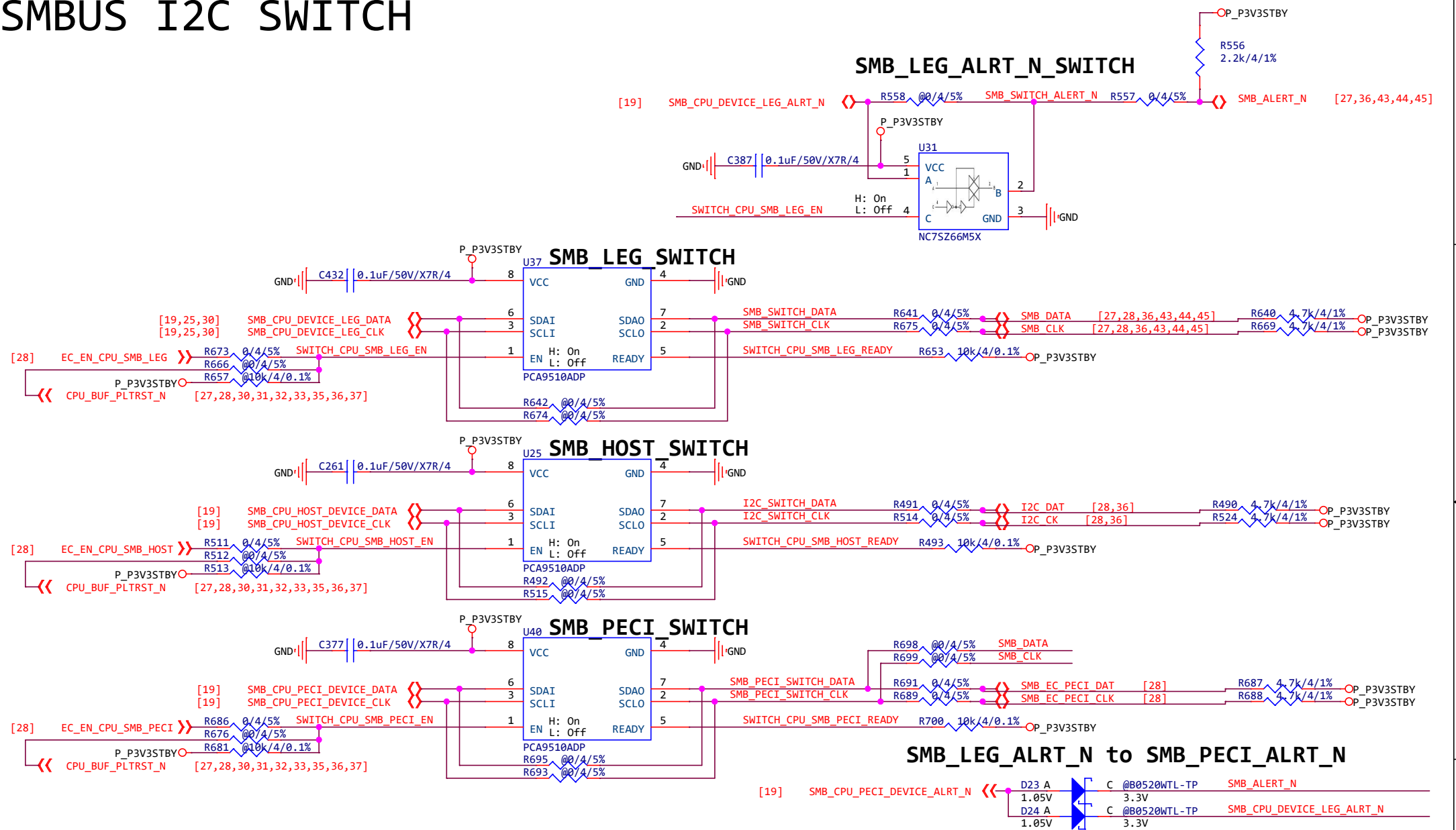
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QMS Number: FMA-HW01008-01 R01

Model Name		CPUC_DVN-0619-ZZ		Rev	0B
Size	Page Name	32_LPC_CLK_BUFFER_SERIRQ		Engineer	
A					
Date:	Wednesday, January 06, 2021	Sheet	32	of	50

SMBUS I2C SWITCH



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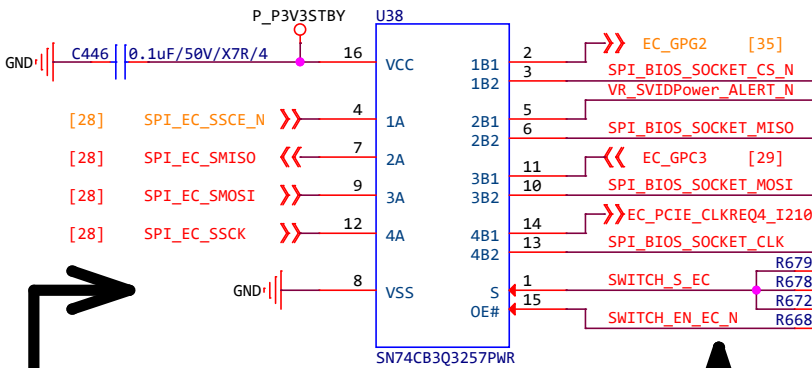
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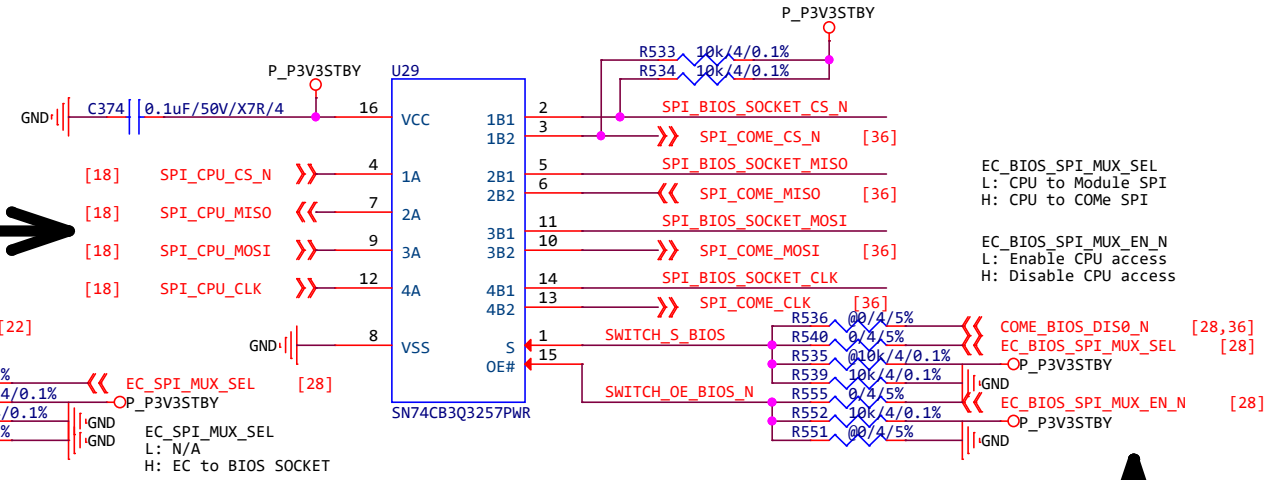
Model Name		CPUC_DVN-0619-ZZ	Rev	0B
Size	Page Name	Engineer		
A	33_SMBUS_I2C_SWITCH			
Date:	Wednesday, January 06, 2021	Sheet	33	of 50

BIOS EC SPI FLASH

[44] VR_Pin_ALERTB_VDDQ_PVNN
[45] VR_Pin_ALERTB_PVCCCPU_PVCCRAM

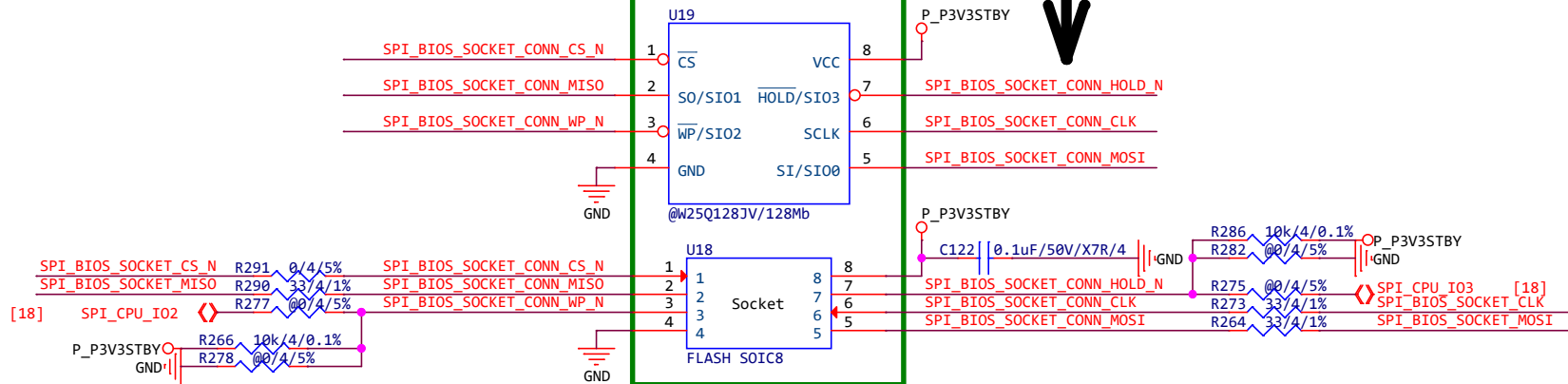


CPU



SPI_BIOS_SOCKET

Co-layout



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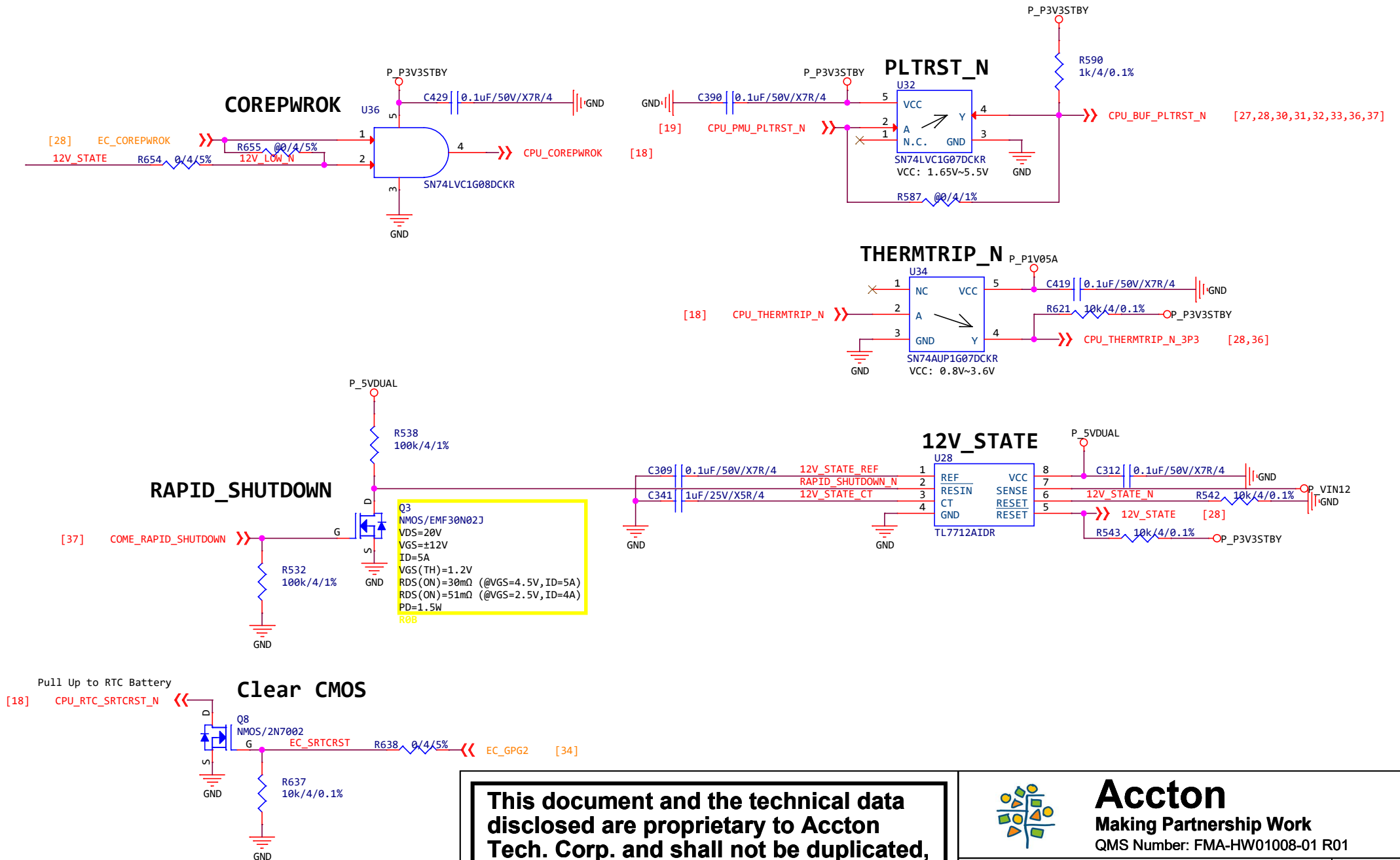
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QMS Number: FMA-HW01008-01 R01

Model Name CPUC_DVN-0619-ZZ			Rev 0B
Size A	Page Name 34_BIOS_EC_SPI_FLASH	Engineer	
Date: Wednesday, January 06, 2021	Sheet 34	of 50	

HW Logic



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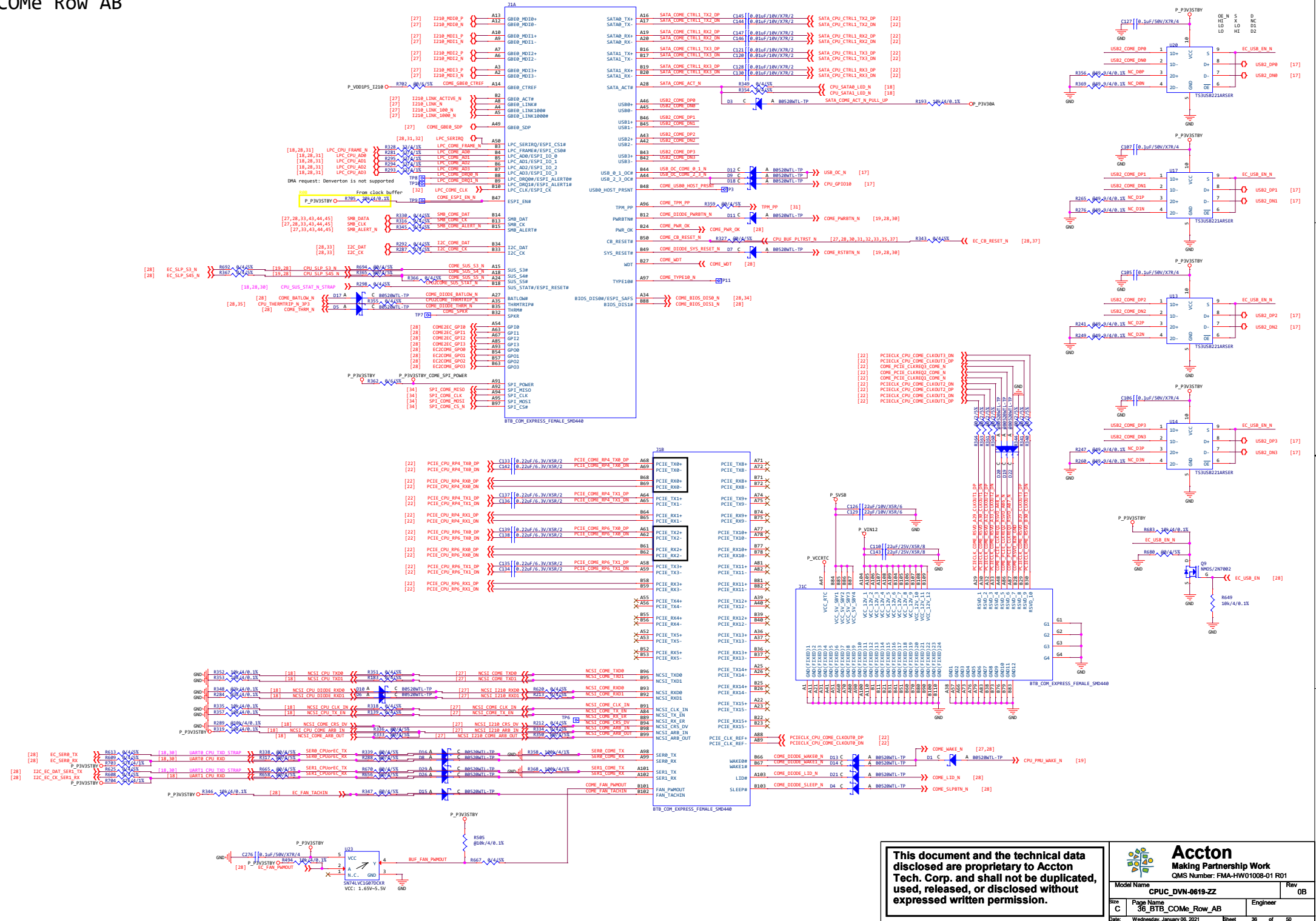
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QMS Number: FMA-HW01008-01 R01

Model Name		Rev
CPUC_DVN-0619-ZZ		0B
Size	Page Name	Engineer
A	35_HW_Logic	
Date:	Wednesday, January 06, 2021	Sheet 35 of 50

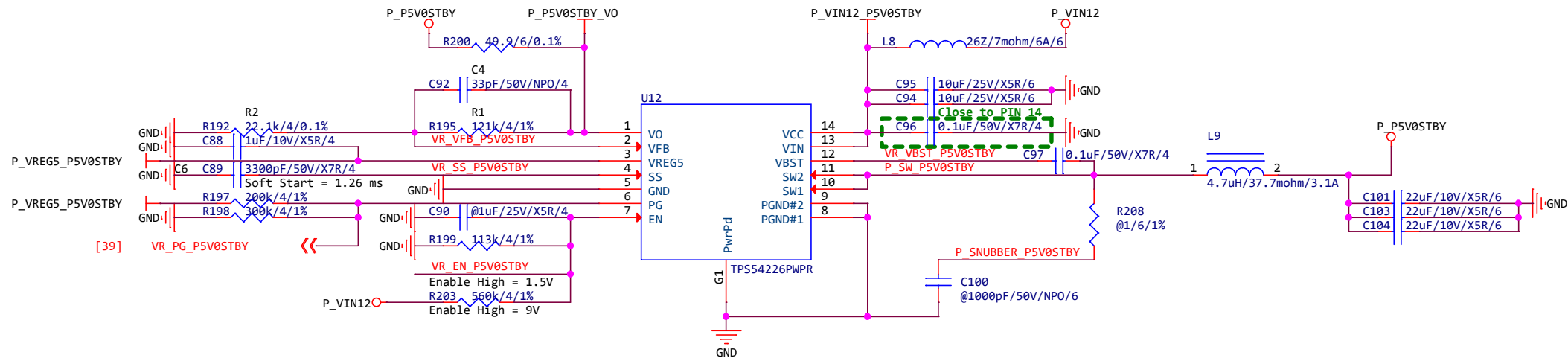
COMe Row AB



[illegible]

 Accton Making Partnership Work QMS Number: FMA-HW01008-01 R01					
<table border="1"> <tr> <td>Model Name</td> <td>CPUC_DVN-0619-ZZ</td> <td>Rev</td> <td>0B</td> </tr> </table>		Model Name	CPUC_DVN-0619-ZZ	Rev	0B
Model Name	CPUC_DVN-0619-ZZ	Rev	0B		
Size	<table border="1"> <tr> <td>Page Name</td> <td>37_BTB_COME_Row_CD</td> <td>Engineer</td> <td></td> </tr> </table>	Page Name	37_BTB_COME_Row_CD	Engineer	
Page Name	37_BTB_COME_Row_CD	Engineer			
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P5V0STBY



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Model Name		CPUC_DVN-0619-ZZ		Rev	0B
Size	Page Name	38_P5V0STBY		Engineer	
A					
Date:	Wednesday, January 06, 2021	Sheet	38	of	50



1

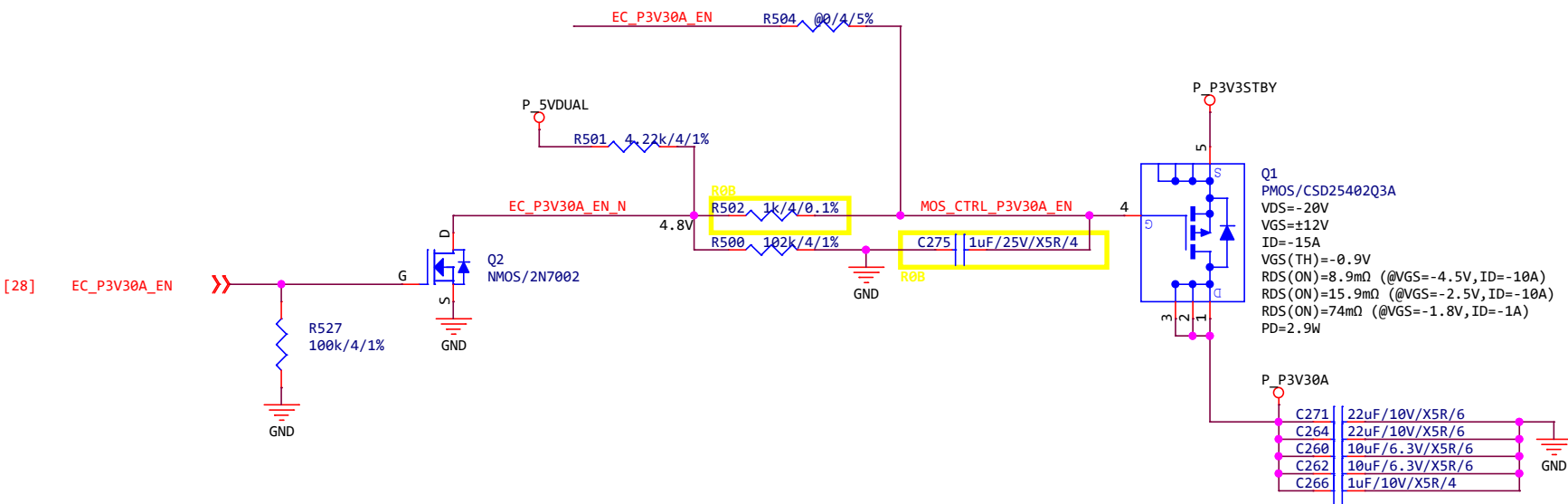


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P3V30A



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QMS Number: FMA-HW01008-01 R01

Model Name		Rev
CPUC_DVN-0619-ZZ		0B
Size	Page Name	Engineer
A	41_P3V30A	
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P_P3V3STBY

P_P3V3STBY_P1V80A

P_P1V80A

C350 10uF/25V/X5R/6

C362 10uF/25V/X5R/6

L25 26Z/7mohm/6A/6

GND

P_P3V3STBY

C84 4.7uF/10V/X5R/4

Close to PIN 4

[28] EC_EN_P1V80A

R190 100k/4/1%

GND

C80 560pF/50V/X7R/4

VR_SS_P1V80A

U10 TPS74901DRCR

IN1

IN2

OUT1

OUT2

BIAS

FB

EN

PG

SS

TH_PAD

GND

C321 22uF/10V/X5R/6

C311 22uF/10V/X5R/6

C323 22uF/10V/X5R/6

C335 10uF/6.3V/X5R/6

GND

R180 3.57k/4/1%

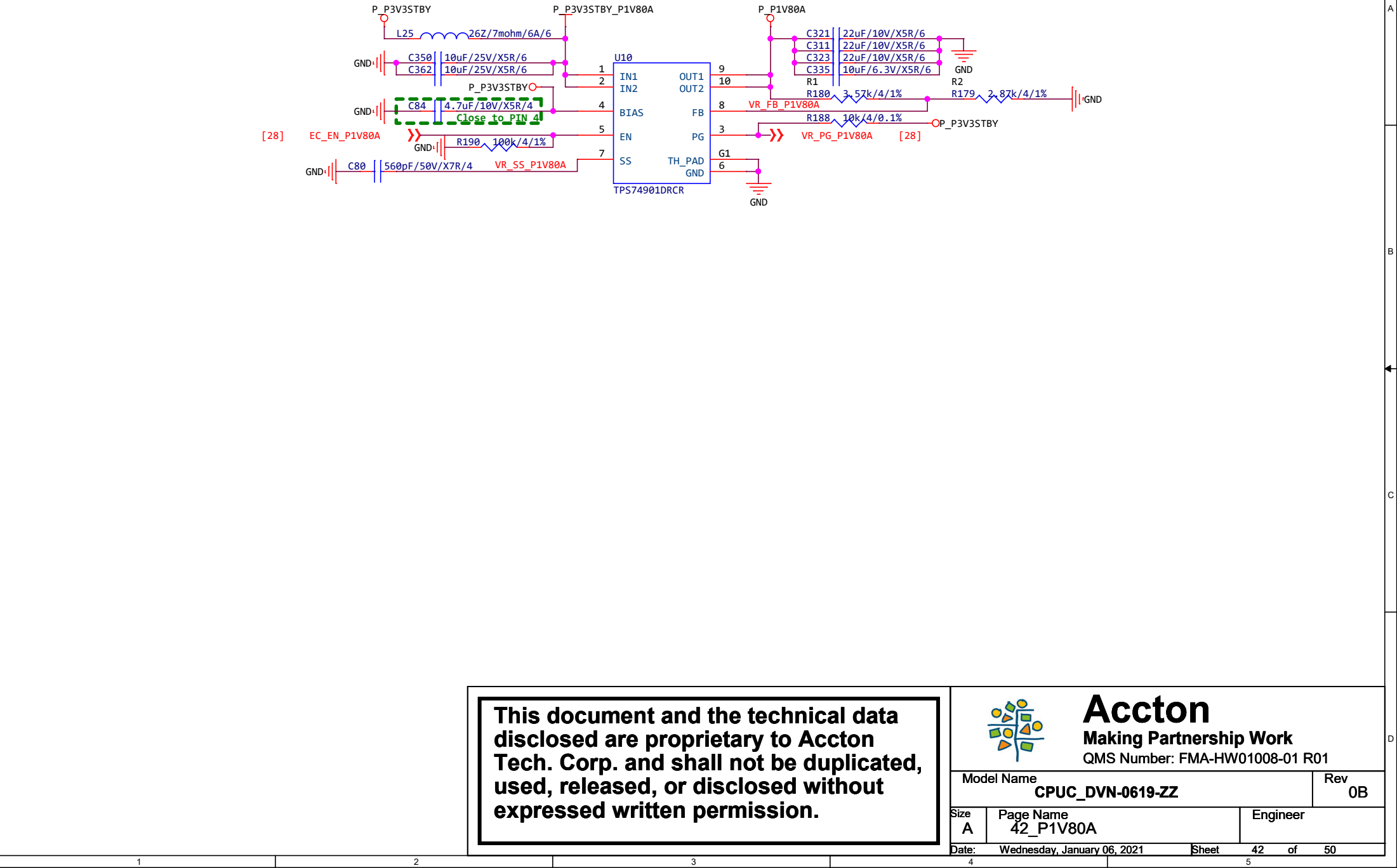
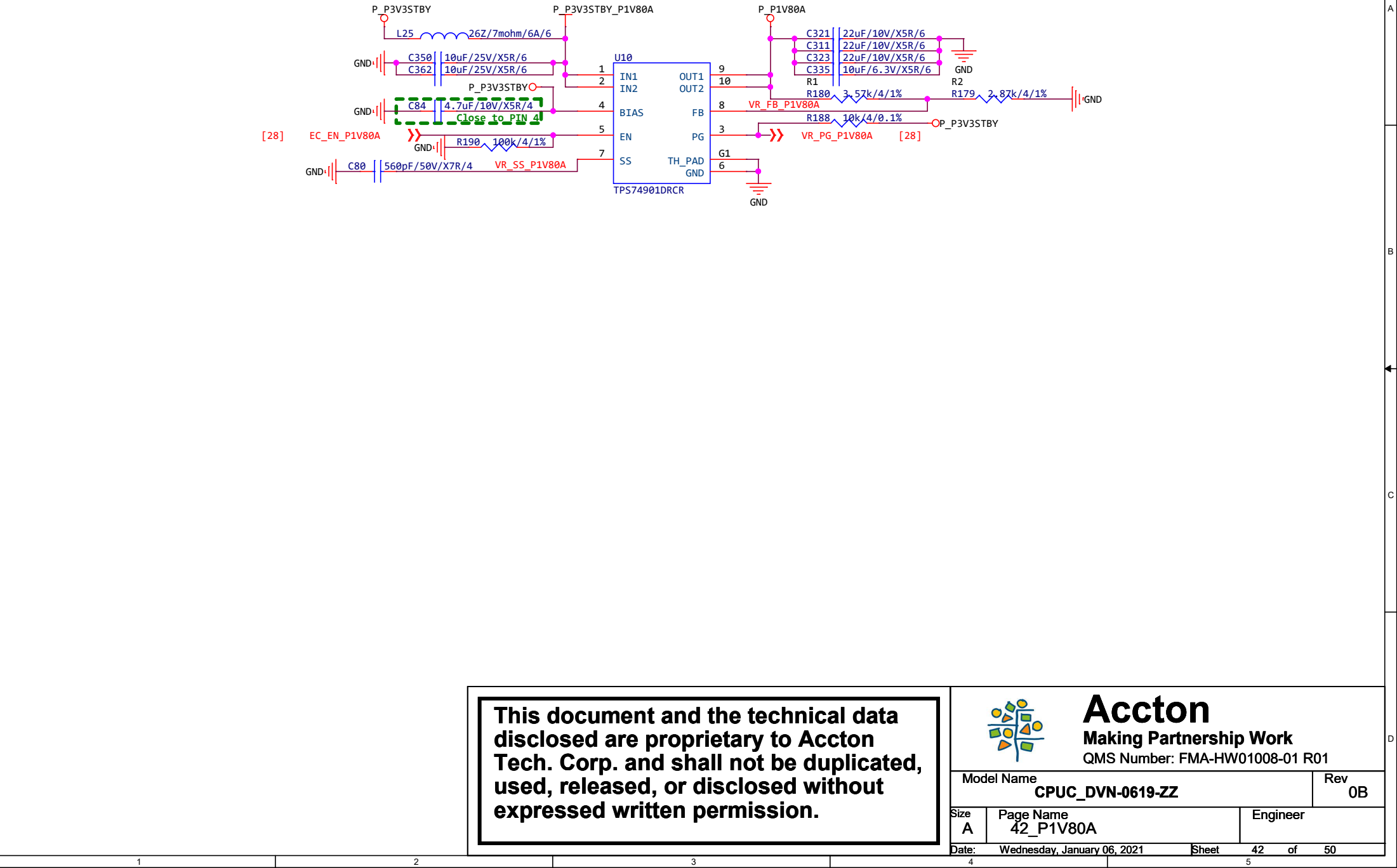
R179 2.87k/4/1%

VR_FB_P1V80A

R188 10k/4/0.1%

OP_P3V3STBY

[28] VR_PG_P1V80A

[illegible]

The schematic diagram illustrates the internal circuitry of a TPS74901DRCR voltage regulator. The central component, U10, is a precision centrobuck converter. Its input is connected to a network of capacitors (C350, C362) and an inductor (L25) to filter the input voltage. The feedback loop is established by a resistor divider (R180, R188) connected to the FB pin, which is also tied to the BIAS pin. The output voltage is regulated by the feedback network and the internal error amplifier. The output filter consists of a capacitor (C321, C311, C323, C335) and a resistor (R179) to provide low-impedance regulation. The circuit is powered by a 3.3V input (P_P3V3STBY) and regulated to 1.8V (P_P1V80A). The output is connected to a power plane (P_P1V80A) and a ground plane (GND). The diagram also shows various test points and connections for the regulator's pins, including IN1, IN2, OUT1, OUT2, BIAS, FB, EN, PG, SS, TH_PAD, and GND.

Legend:

- U10:** TPS74901DRCR
- C350, C362:** 10uF/25V/X5R/6
- L25:** 26Z/7mohm/6A/6
- C321, C311, C323, C335:** 22uF/10V/X5R/6
- R180, R188, R179:** 3.57k/4/1%, 10k/4/0.1%, 87k/4/1%
- R190:** 100k/4/1%
- C84:** 4.7uF/10V/X5R/4
- C80:** 560pF/50V/X7R/4

Power Planes and Grounds:

- P_P3V3STBY:** Input power plane
- P_P3V3STBY_P1V80A:** Intermediate power plane
- P_P1V80A:** Output power plane
- EC_EN_P1V80A:** Enable signal
- VR_SS_P1V80A:** Sense signal
- VR_FB_P1V80A:** Feedback signal
- VR_PG_P1V80A:** Power good signal
- GND:** Ground

Pin Connections:

- IN1:** Connected to P_P3V3STBY
- IN2:** Connected to P_P3V3STBY_P1V80A
- OUT1:** Connected to P_P1V80A
- OUT2:** Connected to P_P1V80A
- BIAS:** Connected to FB
- FB:** Connected to FB
- EN:** Connected to EC_EN_P1V80A
- PG:** Connected to VR_PG_P1V80A
- SS:** Connected to VR_SS_P1V80A
- TH_PAD:** Connected to GND
- GND:** Connected to GND

[illegible]

P_P3V3STBY

L25 26Z/7mohm/6A/6

GND

C350 10uF/25V/X5R/6

C362 10uF/25V/X5R/6

P_P3V3STBY

GND

C84 4.7uF/10V/X5R/4

[28] EC_EN_P1V80A

GND

C80 560pF/50V/X7R/4

VR_SS_P1V80A

P_P3V3STBY_P1V80A

U10

IN1

IN2

OUT1

OUT2

BIAS

FB

EN

PG

SS

TH_PAD

GND

TPS74901DRCR

P_P1V80A

C321 22uF/10V/X5R/6

C311 22uF/10V/X5R/6

C323 22uF/10V/X5R/6

C335 10uF/6.3V/X5R/6

R1

R180 3.57k/4/1%

R179 2.87k/4/1%

R178 2.87k/4/1%

VR_FB_P1V80A

R188 10k/4/0.1%

OP_P3V3STBY

[28]

VR_PG_P1V80A

GND

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Model Name CPUC_DVN-0619-ZZ		Rev 0B
Size A	Page Name 42_P1V80A	Engineer
Date: Wednesday, January 06, 2021		Sheet 42 of 50

P_P3V3STBY

P_P3V3STBY_P1V80A

P_P1V80A

C350 10uF/25V/X5R/6

C362 10uF/25V/X5R/6

L25 26Z/7mohm/6A/6

GND

P_P3V3STBY

C84 4.7uF/10V/X5R/4

Close to PIN 4

[28] EC_EN_P1V80A

R190 100k/4/1%

GND

C80 560pF/50V/X7R/4

VR_SS_P1V80A

U10 TPS74901DRCR

IN1

IN2

OUT1

OUT2

BIAS

FB

EN

PG

SS

TH_PAD

GND

C321 22uF/10V/X5R/6

C311 22uF/10V/X5R/6

C323 22uF/10V/X5R/6

C335 10uF/6.3V/X5R/6

R1 3.57k/4/1%

R180 3.57k/4/1%

R188 10k/4/0.1%

R179 2.87k/4/1%

GND

VR_FB_P1V80A

VR_PG_P1V80A

[28]

P_P3V3STBY

P_P3V3STBY

P_P3V3STBY_P1V80A

P_P1V80A

C350 10uF/25V/X5R/6

C362 10uF/25V/X5R/6

L25 26Z/7mohm/6A/6

GND

P_P3V3STBY

C84 4.7uF/10V/X5R/4

Close to PIN 4

[28] EC_EN_P1V80A

R190 100k/4/1%

GND

C80 560pF/50V/X7R/4

VR_SS_P1V80A

U10 TPS74901DRCR

IN1

IN2

OUT1

OUT2

BIAS

FB

EN

PG

SS

TH_PAD

GND

C321 22uF/10V/X5R/6

C311 22uF/10V/X5R/6

C323 22uF/10V/X5R/6

C335 10uF/6.3V/X5R/6

GND

R180 3.57k/4/1%

R179 2.87k/4/1%

GND

VR_FB_P1V80A

R188 10k/4/0.1%

OP_P3V3STBY

[28] VR_PG_P1V80A

P_P3V3STBY

P_P3V3STBY_P1V80A

P_P1V80A

C350 10uF/25V/X5R/6

C362 10uF/25V/X5R/6

L25 26Z/7mohm/6A/6

GND

P_P3V3STBY

C84 4.7uF/10V/X5R/4

Close to PIN 4

[28] EC_EN_P1V80A

R190 100k/4/1%

GND

C80 560pF/50V/X7R/4

VR_SS_P1V80A

U10 TPS74901DRCR

IN1

IN2

OUT1

OUT2

BIAS

FB

EN

PG

SS

TH_PAD

GND

C321 22uF/10V/X5R/6

C311 22uF/10V/X5R/6

C323 22uF/10V/X5R/6

C335 10uF/6.3V/X5R/6

GND

R180 3.57k/4/1%

R179 2.87k/4/1%

GND

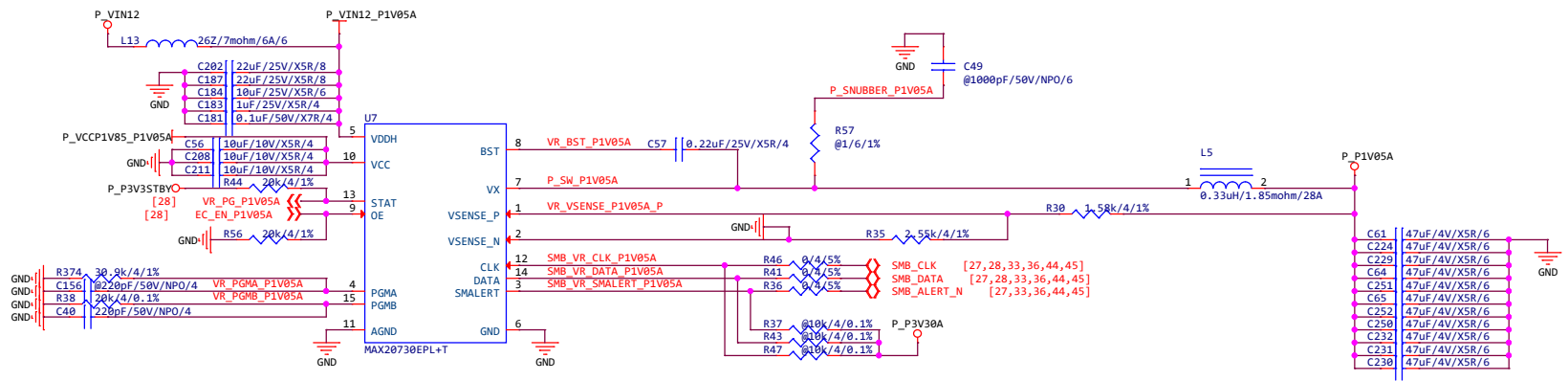
VR_FB_P1V80A

R188 10k/4/0.1%

OP_P3V3STBY

[28] VR_PG_P1V80A

P1V05A



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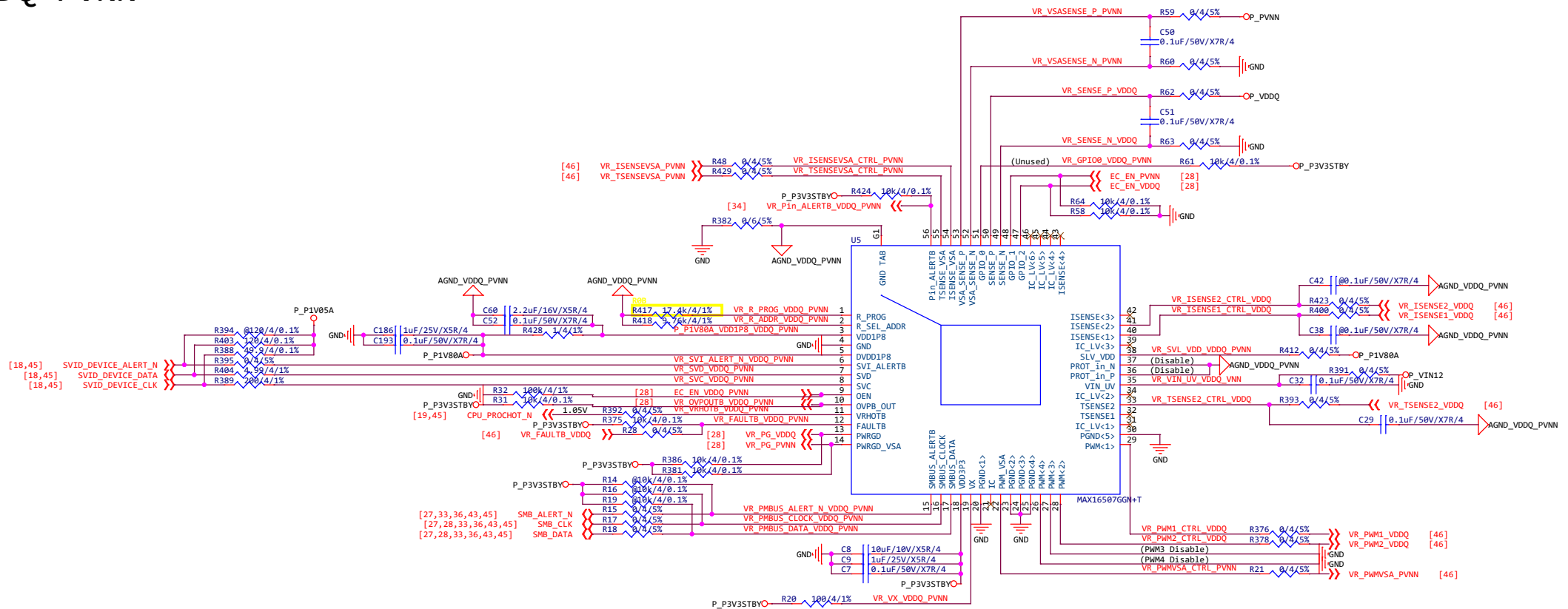


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QMS Number: FMA-HW01008-01 R01

Model Name CPUC_DVN-0619-ZZ		Rev 0B
Size B	Page Name 43_P1V05A	Engineer
Date: Wednesday, January 06, 2021		Sheet 43 of 50

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QMS Number: FMA-HW01008-01 R01

The schematic diagram illustrates the power supply network for the PVNN board. It shows three main input rails: P_VEN12, P_VEN12_PVNN, and P_VEN12_PVNN. The P_VEN12 rail is connected to a 1A current source L11 (2x2mm/6A/6). The P_VEN12_PVNN rail is connected to a 0.22µF capacitor C39 (0.22µF/25V/XSR/4) and a 1.8Ω resistor R1. The P_VEN12_PVNN rail is also connected to a 0.1µF capacitor C175 (0.1µF/25V/XSR/8), a 1µF capacitor C159 (1µF/50V/XTR/6), and a 1µF capacitor C3 (1µF/50V/XTR/6). The P_VEN12_PVNN rail is connected to a 1µF capacitor C159 (1µF/50V/XTR/6), a 4.7nF capacitor C167 (4.7nF/50V/XTR/6), and a 470nF capacitor C157 (470nF/50V/XTR/4). The P_VEN12_PVNN rail is connected to a 0.1µF capacitor C21 (0.1µF/50V/XTR/4) and a 0.1µF capacitor C2 (0.1µF/50V/XTR/4). The P_VEN12_PVNN rail is connected to a 0.1µF capacitor C21 (0.1µF/50V/XTR/4) and a 0.1µF capacitor C2 (0.1µF/50V/XTR/4). The P_VEN12_PVNN rail is connected to a 0.1µF capacitor C21 (0.1µF/50V/XTR/4) and a 0.1µF capacitor C2 (0.1µF/50V/XTR/4).

CPU



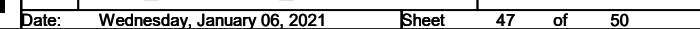
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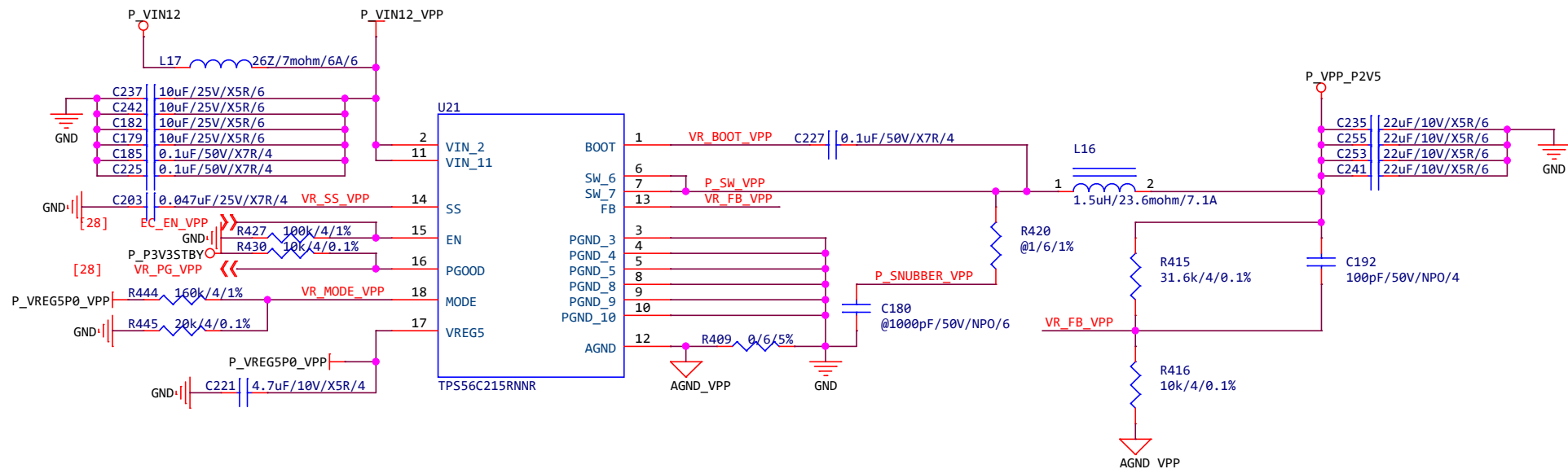
QMS Number: FMA-HW01008-01 R01

Model Name	CPUC_DVN-0619-ZZ	Rev	0B
Size	Page Name	Engineer	
C	46 Power_Stage		
Date	Wednesday, January 08, 2021	Sheet	46 of 50

1	2	3	4	5
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VPP_P2V5



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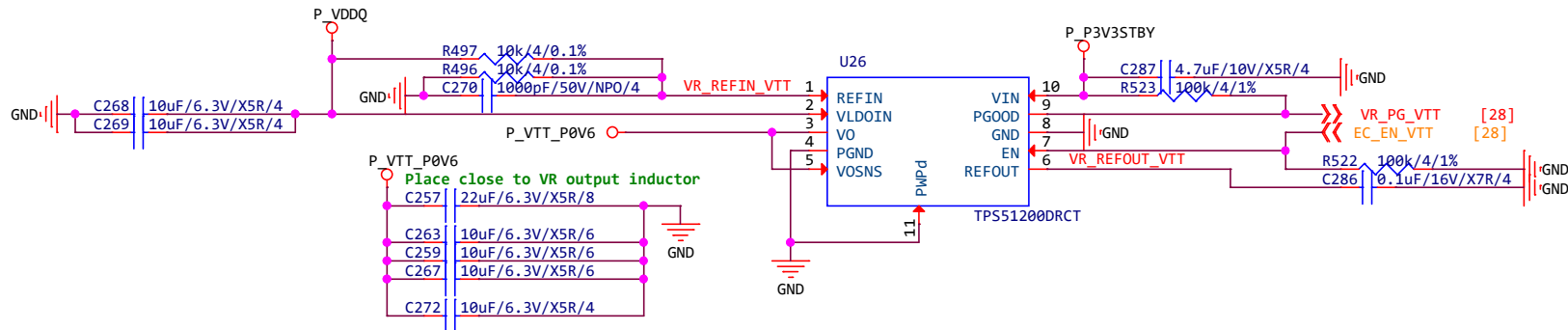
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QMS Number: FMA-HW01008-01 R01

Model Name		Rev	
CPUC_DVN-0619-ZZ		0B	
Size	Page Name	Engineer	
A	27_VPP_P2V5		
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VTT_P0V6



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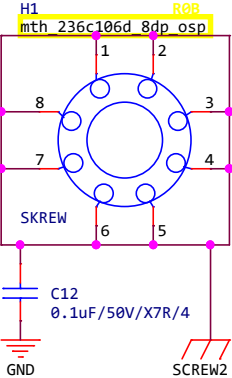
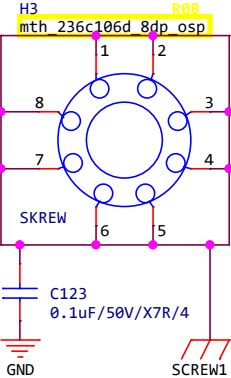
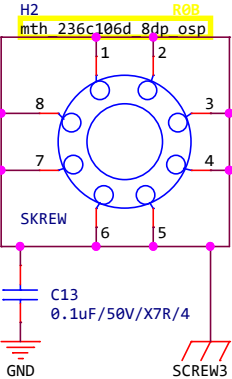
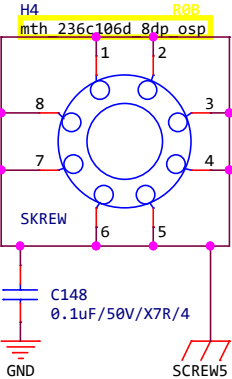
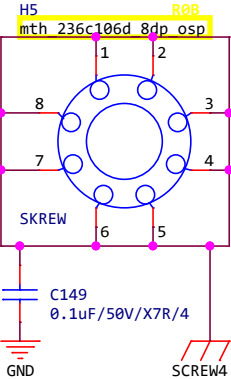
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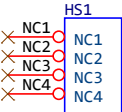
QMS Number: FMA-HW01008-01 R01

Model Name		Rev
CPUC_DVN-0619-ZZ		0B
Size	Page Name	Engineer
A	22_VTT_P0V6	
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Mounting Hole



Heatsink



76mm
Part Number = 117200000797A
Description = ?!HEATSINK 94.24X76X12.85mm SILVER AL1050 SCREW4 AURAS
PCB Footprint = hsink_38dx56d_4dnp_94d24w76l
Package Type = 0

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QMS Number: FMA-HW01008-01 R01

Model Name		Rev	
CPUC_DVN-0619-ZZ		0B	
Size	Page Name	Engineer	
A	16_Mounting_Hole_and_Heatsink		
Date:	Wednesday, January 06, 2021	Sheet	50 of 50